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STUDY AND DEVELOPMENT OF MICROELECTRONICS APPLICATION SPECIFIC INTEGRATED CIRCUITS (ASICs) CHIPS FOR THE READOUT OF DETECTORS

Thesis

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Nous, Professeurs **BODO Bertrand, MBINACK Clément** et Professeur **WOAFO Paul**, respectivement Examinateurs et Président du Jury de la thèse de **Doctorat/PhD** de Monsieur **FOLLA KAMDEM Jérôme** Matricule **13T2172**, préparée sous la direction du Professeur **WEMBE TAFO Evariste** et sous la supervision du Professeur **ESSIMBI ZOBO Bernard**, intitulée : « **STUDY AND DEVELOPMENT OF MICROELECTRONICS APPLICATION SPECIFIC INTEGRATED CIRCUIT CHIPS FOR THE READOUT OF DETECTORS**», soutenue le **Vendredi, 17 Décembre 2021**, en vue de l'obtention du grade de **Docteur/Ph.D** en Physique, Spécialité **Systèmes Electriques et Electroniques**, attestons que toutes les corrections demandées par le Jury de soutenance ont été effectuées.

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Fait à Yaoundé le 05 JAN 2022

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Ndjaka Jean-Marie Bienvenu
Professeur

DEDICATION

To

My lovely mother born DJINEKOU Marie

My late father KAMDEM INNOCENT

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List of abbreviations

AC: Alternative Current

ADC: Analog to Digital Converter

AFD: Analog Front-End

ASIC: Application Specific Integrated Circuit

CMOS: Complementary Metal Oxide Semiconductor

CSA: Charge Sensitive Amplifier

CMS: Compact Muon Solenoid

CLTF: Closed-loop transfer function

DAC: Digital to Analog Converter

DAQ: Data Acquisition

DC: Direct Current

DD: Displacement Damage

DILB: Drain Induced Barrier Lowering

DLC: Dynamic Latch Comparator

DPP: Digital Pulse Processing

DSP: Digital Signal Processor

ECG: Electro-Cardiogram

EEG: Electro-Encephalogram

ECoG: Electro-Corticograms

ENC: Equivalent Noise Charge

FEE: Front-End Electronics

FPGA: Field Programmable Gate Array

FWHM: Full Width Half Maximum

GBP: Gain-Bandwidth product

HEPE: High Energy Physics Experiment

HLC: Large Hardron Collider

IC: Integrated Circuit

ICTP: International Centre for Theoretical Physics

OLTF: Open-loop transfer function

LOR: Line of Response

MOS: Metal Oxide Semiconductor

MOSFET: Metal Oxide Field Effect Transistor

NMOSFET: N-channel Metal Oxide Field Effect Transistor

PC: Personal Computer

PMOSFET: P-channel Metal Oxide Field Effect Transistor

MPA: Macro Pixel ASIC

MLAB: Multidisciplinary Laboratory

PET: Positron Emission Tomography

PM: Phase Margin

PSD: Position Sensitive Detector

PS: Pulse Shaper

PVT: Process Voltage and Temperature

VLSI: Very Large Scale Integration Systems

SEE: Single Event Effects

SEL: Single Event Latch-up

SSA: Short Strip ASIC

SNR: Signal-to-Noise Ratio

SoC: System-on-Chip

SDD: Silicon Drift Detectors

STI: Shallow Trench Isolation

VHDL: Very high scale Hardware Description Language

VLSI: Very Large Scale Integration System

RAM: Random Access Memory

RINCEs: Radiation-Induced Narrow Channel Effects

ROM: Read Only Memory

ROIC: Readout integrated Circuits

RRL: Ripple Rejection Loop

EEPROM: Electrically Erasable Programmable Read Only Memory

TDC: Time to Digital Converter

TSMC: Taiwan Semiconductor Manufacturing Company

ABSTRACT

This thesis deals with the study and development of microelectronics and application specific integrated circuits (ASICs) chip for the readout of detectors. The main target detectors are pixel-strip and small capacitive silicon based detectors for X-rays and gamma rays applications. The fundamentals of readout ASICs in radiation detection systems have been studied. Based on this, general architecture of those readout systems is described. For particles tracking and energy measurement the readout chip is built of an analog front-end for particles extraction and filtering and a digital unit to acquire the filtered data.

The analog Front-End application specific integrated circuit chip (ASIC) is made of a charge sensitive amplifier (CSA), a first order pulse shaper which output is triggered by a fast discriminator module based dynamic latch comparator. The CSA being the key element of the design, mathematical analysis based small signal model of its core amplifier has been performed to guarantee high dc-gain which helps in preventing fast particles collection process and wide bandwidth to handle large number of pileup events. Based on this, the design parameters for a low-noise, low-power and stable FE-ASIC has been identified. Transistor level design of the circuit was performed to exhibit an internal gain stage controlled by an external device; giving therefore more flexibility to a user to control the incoming particles flux rate. The input transistors of the CSA and the PS modules have been optimized in terms of channel width, transconductance and drain current. The radiation hardness behavior of spectroscopic front-end electronics (FEE) being affected by the equivalent noise charge (ENC) of the device, namely considered as the parameter that embodies the noise in spectroscopic front-end derives; the ENC of our circuit was well analyzed and optimized with regards to the detector capacitance and circuit parameters. We explore therefore, the effects of each design parameter on the ENC and discussed the possibility of enlarging the incoming particles flux while operating in low-power and low-noise conditions. The radiation tolerant behavior of the circuit was analyzed, giving therefore the opportunity to discuss its amplitude resolution. In addition, we analyzed the pulse shape discrimination strategy of the proposed ASIC. Considering that in silicon based detectors spectroscopy, the particles arrival time is a crucial element for photon tracking and energy measurement. The output of the PS is delayed while discriminating the signals and it results in

false photon detection and loss of energy, which worsen the detection efficiency. Considering this, an ultra-fast dynamic latch comparator was designed to minimize the detection delay. We find out that incoming particles can be trigger with a maximum clock rate of 20 GS/s with less than 15 ps time delay; giving therefore the possibility of handling big amount of data while detecting particles with high transverse momentum.

This work contributes to the understanding of single photon detection and processing systems. Moreover, it helps to bring our solution to the issue of energy lost, power dissipation and detection efficiency which is encountered in modern silicon based detector front-end ASICs.

Keywords: Front-End ASIC, CMOS technology process, counting rate, discriminator, high energy physics, radiation detection systems, silicon based detector applications.

RÉSUMÉ

Cette thèse porte sur l'étude et le développement d'une électronique intégrée de type 'applications spécifiques integrated circuits (ASIC)' pour la lecture de détecteurs. Les principaux détecteurs ciblés dans notre étude sont des détecteurs semiconducteurs capacitifs à pistes et à pixels à base de silicium, utilisés pour des applications à rayons X/gamma. Fort des fondamentaux sur les circuits de lecture dans les systèmes de détection des radiations, les différentes architectures des ASICs utilisés dans lesdits circuits de lectures ont été étudiées. Pour la mesure de la trajectoire et l'énergie des particules, le système de lecture est constitué d'une électronique analogique frontale pour l'extraction des charges, l'amplification et le filtrage des signaux extraits puis d'une unité numérique pour l'acquisition des signaux filtrés.

L'électronique analogique frontale de type ASIC est constituée d'un amplificateur sensible à la charge (PSC), d'un filtre analogique de premier ordre ou pulse shaper (PS) dont la sortie est discriminée par un comparateur à verrouillage dynamique, circuit principal du module discriminateur. Le PSC étant l'élément clé du circuit analogique, une analyse de son modèle de petits signaux a été faite, permettant de garantir un gain en courant continu suffisamment ; ce qui permet de réduire le temps de collecte des charges, élargir la bande passante et partant gérer un flux important de particules incidents. Sur ce, les paramètres de conception d'un ASIC stable et faible bruits qui a les avantages de consommer une faible puissance ont été identifiés. La conception niveau transistors du circuit a été faite permettant d'intégrer un étage amplificateur dont le gain est commandé par un dispositif externe ; donnant ainsi la possibilité à tout utilisateur externe de contrôler la bande passante du circuit et partant le débit des particules détectées. Les paramètres géométriques et électriques des transistors d'entrée des modules PSC et PS ont été optimisés à savoir la largeur du canal, la transconductance et le courant de drain. La robustesse aux radiations étant fonction du bruit équivalent charge ou 'equivalent noise charge (ENC)' l'ENC de notre circuit a été bien analysé, modélisé et optimisé en fonction de la capacité du détecteur ; de la largeur du canal du courant de drain du transistor d'entré du PSC. Nous avons exploré par la suite les effets de chacun de ces paramètres sur l'ENC et avons discuté de la possibilité de traiter un flux de particules élevé tout en préservant la puissance et la résolution énergétique de notre système. Par la suite, nous avons analysé la stratégie de discrimination des impulsions provenant du module analogique de l'ASIC proposé. Considérant qu'en spectroscopie des détecteurs à base de silicium, le

temps d'arrivée des particules est un élément crucial pour la détection des photons et la mesure de leur énergie. La sortie du PS est retardée lors de la discrimination des signaux et il en résulte une détection de faux photons et une perte d'énergie, ce qui détériore l'efficacité de détection. Compte tenu de cela, un comparateur à verrouillage dynamique ultra-rapide a été conçu pour minimiser le délai de détection. Nous découvrons que les particules entrantes peuvent être discriminées avec une fréquence d'horloge maximale de 20 GS/s pour un délai inférieur à 15 ps ; donnant ainsi la possibilité de traiter une grande quantité de données tout en détectant des particules ayant un moment transversal de plus de 2 GeV/c.

Ces travaux apportent une contribution à l'amélioration du fonctionnement de la chaine de détection et de traitement des particules émises par les détecteurs à semi-conducteurs. Nous apportons de ce fait, une solution aux problèmes de perte d'énergie, de résistance aux radiations et de puissance dissipée rencontrés dans les détecteurs modernes utilisés en Physique des particules en industrie et dans le domaine médicale.

Mots clés: ASIC, électronique frontale analogique, physique des particules, Technologie CMOS, système de détection de photon, détecteur à base de silicium, retard.

GENERAL INTRODUCTION

The interaction mechanisms between particles and matter are both at the basis of the working principles of semiconductor detectors and microelectronics systems developed for scientific and industrial applications. Electronic circuits and systems are employed in a number of different fields where some degree of radiation tolerance is required. These fields include high-energy physics experiments, nuclear and thermonuclear power plants, medical diagnostic imaging and therapy [1-7]. When operated in these environments, the electronic systems may be directly struck by particles or highly energetic photons, with a subsequent alteration of their electrical properties. Therefore, these electronics systems have to comply with severe requirements in terms of low-noise, low-power, high-speed operations and high radiation tolerance.

Readout integrated circuits (ROICs) have become the most important way for extracting low particles charge or current into semiconductor detectors [1, 2, 8 and 9]. They perform precise measurement of particles energy, trajectories and moment, by amplifying the output signal of the photon sensor [1-10]. A data acquisition (DAQ) block based FPGA then extracts information about the photons, such as position, energy, time and momentum, from the output signals of the readout electronics and uses it to find a coincidence pair of photons to create a line of response (LOR) [9-16]. For instance, the Compact Muon Solenoid (CMS) is foreseen to receive a substantial upgrade of the outer tracker sensor and its front-end readout electronics, requiring higher granularity and readout bandwidth to handle the large number of pileup events in the High-Luminosity LHC [6, 8 and 9], [17-22]. For this reason, the entire tracking system will be replaced with new sensors featuring higher radiation tolerance and ability to handle higher readout bandwidths and data rates [2, 4]. To identify particles with high transverse momentum (> 2 GeV/c) and to distinguish the front-end output with a given L1 trigger level, a double layer sensor module, which combines a pixel sensor with a strip one, was adopted. Consequently, two different readout ASICs were developed, namely the Short Strip ASIC (SSA) for the strip sensor and the Macro Pixel ASIC (MPA) for the pixilated sensor [23-26]. To readout the sensors hits and locally process and compress higher particles flux, the readout electronics of the SSA is needed to be implemented within a complementary metal oxide semiconductor (CMOS) technology process and integrated to the

sensor chip [1-7]. This requires low power and radiation-hard analog Front-End (AFE) totally implemented within a CMOS technology [25-28].

Recent studies on ROICs for capacitive radiation detectors let appear special behaviors having applications in fundamental science, technology and medicine [1, 2, 3, 8 and 9]. In the particular case of silicon-based detectors, numerous studies have been carried out [29-32]. Typical biosensor devices and nuclear instruments include custom-made sensing electronics. Many of those sensing systems must be further supported with a system of electronics and/or software to supply the end user with meaningful data and a useable interface. In many implementations, designing or even setting up the supporting electronic hardware can become more involved or time consuming than the detection device its self. With discrete devices, external detection hardware is often used due to the readily available forms of computer video recording devices for CCD/CMOS video-based sensors [28, 30, 33 and 34], and the wide range of computer-interfaced systems. These readily available interfaces have some limitations, including their size, lack of portability, lack of spatial resolution, and need of trained personnel with appropriate laboratory facilities [28, 30 and 35]. In most of those cases, the integrated solutions include front-end modules, such as a charge, sensitive amplifier and shaping amplifier for both photodiode based light detectors and implantable biomedical sensors. Including the sensor and detection electronics on a single chip or package with either a wired or a wireless interface simplifies the use of the biosensor in research, and allows for greater complexity in hardware implementation [34-38]. With an integrated front-end system, a user could easily connect an array of thousands of electrodes to a computer for data acquisition using a single connector or wireless interface, eliminating the need for highly trained personnel and bulky hardware. However, this issue is usually suffered from more power dissipation, more noise and occupied more die area [1, 2], [39-42].

Review on silicon based detectors Front-End ASICs module

Recent research on pixel-strip sensors reveals that those devices can transform gamma rays to charges operating at normal temperature, which exhibits a better potentiality for the detection of X-rays and γ-rays for possible nuclear instrumentation applications [6]. A typical thickness for Si-sensor is about 300 µm; the limiting irradiation energy, which would penetrate protons through the sensor, is about 6.2 MeV [5, 7]. In contrast to spectroscopic amplifiers, the major concerned for fast amplifiers is the preservation of the charge collection process (fast rise time of the signal), in other words, maintaining a wide bandwidth [4]. The improvement of energy resolution leads to optimization of charge collection process by designing the lowest possible rise time of the CSA compared to the peaking time of the shaping amplifier; this would prevent ballistic deficit, which involves loss of resolution.

Therefore, the energy sensitivity of the readout module should be high enough to minimize the energy loss and guarantee the lowest possible rise time (less than 10 ns) while handling higher counting rate operations (more than 1 MHz flux rate) [4]. Moreover, for multi-channel readout electronics, the spatial resolution should be more than 2 µm [4, 5].

A big amount of channels can be made feasible using large-scale integration to include the associated electronics on the same chip of the sensor. Silicon sensors offer a typical signal in the range of tens of thousands of electrons within a collection time of few nanoseconds ROIC processes the signal from the sensor. Signal processing starts with the integration of the input signal, a very small and fast current pulse, into a voltage step performed by CSA [9]. From the signals on the individual CSA, the amplitude of the output voltage is realized. That voltage is proportional to the total integrated charge, which is in time proportional to the energy released by the incident particles in the sensor. This energy must be measured with the highest accuracy and precision [2, 3]. The input node voltage of the CSA increases (tends to increase) and the voltages with the opposite polarity are generated at the output terminal simultaneously.

It is well known that the input signals intercepted by CSA are generally very low. For a source, the generated preamplifier noise and the input impedance of the amplifier influence the front-end noise performance. Therefore, the front-end input stage must ensure that optimum noise matching is achieved for the source impedance. The design parameter of the input stage of CSA directly influences the noise matching. So the equivalent input noise should be kept as low as possible for a given sensor capacitance. A widely accepted front-end design approach is the use of an operational amplifier (Op-amp), with the R-C feedback network. However, this needs large sensor capacitance (about 15 pF), which compromises the stability of the design [6, 12]. The stability, conditions are indicated by the phase margin (PM) and the gain-bandwidth product (GBP) within the Bode plot for the design of single-stage and two-stage amplifiers. However, the stability analysis of multistage amplifiers requires advanced computations than single-or two-stage amplifiers resulting from the existence of complex poles in high-order switch capabilities [6, 16]. In addition, the desirable performance requirements (GBP, PM) rely on the frequency compensation method and the value of the load capacitance. For a complete validation of the front-end electronics with CMOS technology, the overall system specifications are needed [15-17]. In ref [17], H. Wang et al, proposed readout electronics with CSA-based Polyvinylidene Fluoride (PVDF) transducers. The circuit works for low power dissipation and low frequency; but it was prone

to low conversion gain, high feedback capacitance that occupies more die area. Moreover, due to several biasing points, that circuit was prone to more threshold variation and exhibited higher dc-component, which worsen the output swing of the design [18]. In ref [18], Haryong Song et al, proposed the Ripple Rejection Loop (RRL) techniques for mismatch reduction and offset cancellation in the input transistor stage. The technique works for low-frequency applications. However, the RRL circuit for X-rays and gamma-rays spectroscopy could be implemented by the expense of some flicker noise and radiation damage, in high frequency. Moreover, due to power consumption requirements and hit transfer, the on-chip implementation of the RRL circuit is huge and is therefore not encouraged for spectroscopic purpose. A. Baschirotto et al [19], designed a front-end using a single-ended amplifier as CSA stage. The circuit works at high frequency and very low voltage; however, the disadvantages of that circuit are high power consumption and high Equivalent Noise Charge (ENC); furthermore, the circuit was prone to more parallel noise generated by the passive feedback resistor. The main problem in designing nuclear spectroscopy Very Large Scale Integration (VLSI) readout front ends is the execution of low-noise and low-power CSA, which guarantees high particles flux with the lowest pulse pile-up. Therefore, a good choice in the pulse shaping parameters is crucial for achieving good energy resolution and minimum pulse pile-up for high counting rates. For high particles flux experiment, short shaping time (τ_s) reduces the pile-up effects and for an optimal design solution, the minimum τ_s limits the charge collection process and increases the energy resolution accordingly [4, 20]. Therefore, it is necessary to propose an optimal front-end circuit to avoid unnecessary power dissipation and heat in closely packed pixel arrays first avoid. Secondly, the ENC should be optimized with regards to sensor capacitance along with the shaping time and the input transistors width of the CSA and PS module, for performing AC and transient analysis and finally, the core amplifier should guarantee a high loop gain, high stability and very low-power consumption [6]. Beside, the PS output voltage should be accurately discriminated to ensure the lowest possible time delay that could affect the detection of photon events.

Objectives of the Thesis

The problem of power consumption, energy resolution (leads to radiation damage) and particles flux rate still needed to be addressed. Indeed ASICs chip and particularly in X-rays and gamma rays spectroscopy can sometimes be subject to very weak signals ($\sim$ fC charge or

hundred of pico-Amperes current) in a wide noise environment. In such a case, the information of interest (low charge or current) should be extracted and processed until the target host personal computer (PC) [2, 3, 9], [43-46]. It is therefore of interest to study the fundamentals of readout ASIC for radiation detection systems and solid-state detectors for X and γ rays spectroscopy. Since, radiation sensors detect and convert radiation into electric signals [1, 2, 4, 47], the study of signal processing chain is of a particular interest for understanding the characterization and working principle of many electronics devices encountered in various fields of science and technology such as telecommunication, medicine, high energy physics, positron emission tomography (PET) and many more [1, 2, 39, 41, 42 and 43]. This opens the place to the main issue of the present work as "development of a front-end ASIC for the measurement of a charge delivered by a capacitive semiconductor detector with the best possible accuracy compatible with radiations and noise intrinsically present in the amplifying system, and with the constraints set by the different applications (medical implants, High energy Physics measurement and Industry purpose)" [46-50]. It is divided into several objectives as follows:

- Optimizing equivalent noise charge (ENC) in the front-end electronics main block, by custom design of the input transistor. This involves designing a radiation hardened (radiation-tolerant) circuit.
- Optimizing the power consumption in the whole circuit by a proper design of CSA and PS input transistors aspect ratio along with optimizing the shaping time for high flux rate purpose.
- Set an optimal photon arrival time by designing with the highest accuracy the discriminator based on latch type comparator principle.

This development will be based on the previous research works on readout ASICs for single photon detection systems. Beside engineering applications, we expect not only to contribute to the improvement of functioning readout modules encountered in industry (telecommunication devices), in medicine (implantable brain monitoring devices) and high energy physics, but moreover to solve the problem of power consumption, high throughput operations and radiation damage issues which remain a great challenge for technological point of view.

Outline of the Thesis

The Thesis begins with a general introduction. In this introduction, we gave the description of a semiconductor detector readout circuit. The rest of the work is divided into three chapters and organized as follows:

Chapter 1 presents the literature review on readout ASICs for radiation detection. The chapter provides some generalities on ASICs for radiation detectors readout systems. Thereafter, some architectures of readout ASICs used in high-energy physics experiment, medicine and telecommunications are presented, giving the opportunity to discuss about radiation effects on ASICs chip. Besides, detectors technology and some applications of ASICs chip in industry, medicine and high-energy physics experiments are presented. The problem to be solved is therefore recalled at this end.

In chapter 2, a complete ASIC chip for single photon detection systems and photon energy measurement, is described and designed at the transistor-level. The circuit is dedicated to Silicon based detectors where the system guarantees high-energy resolution and high counting rate. The ASIC integrates a wide bandwidth charge sensitive amplifier (CSA) with a fast pulse shaper (PS) which provides the energy deposited in the detector for every detected photon. The PS is followed by a discriminator, which generates the trigger signal when the shaped pulse crosses a turnable threshold voltage reference. The fast discriminator circuit is well discussed and designed based on high-speed dynamic latch comparator (DLC) principle. A particular attention is therefore paid while designing the DLC.

Chapter 3 is devoted to results and discussions of the work. The main results obtained after simulating the different circuits designed in chapter 2 are presented.

In the first part, charge extraction and shaping outcomes for the proposed Front-End ASIC are discussed. We analysed the bandwidth issue of our system along the current biasing stage for bandwidth compensation. Since, the first topology of the CSA was prone to internal feedback, the circuit presents peak pileup issue and offset at the CSA, then the internal feedback issue was solved through small signal analysis model; this allows analysing the main CSA circuit utilized in our proposed ASIC. The transfer function of the improved CSA was simulated based MATLAB tool kit. Thereafter, the spice simulations were carried on to validate the MATLAB based model. The open loop gain and the closed loop gain of the CSA were therefore discussed, then following the pulse shape simulation and energy monitoring of the Front-End ASIC. That allows discussing the charge-to-voltage conversion issue of the circuit, along with the offset and pileup cancellation technique for suitable energy measurement. In the second part, we analysed the noise behavior of our design with a one pulse shaper parameter, giving therefore the opportunity of discussing the optimal designed parameters obtained while optimizing the ENC at the input transistors stage of both the CSA and the shaper circuits. Deep analysis and discussion of the ENC with regards to the different design parameters was

performed. In the third part, the pulse shape discrimination based on fast DLC is discussed. For the purpose, deep analysis of the dynamic latch comparator in terms of time delay, kickback noise, offset voltage, power consumption is performed, and the results are well discussed.

In the last part, attention is paid to the design validation and silicon implementation of the Front-End ASIC. For the purpose, post layout simulations along with process corner analysis of the whole ASIC have been performed and discussed. We also discussed the parasitic and mismatch reduction technique while laying out the design.

Finally, this dissertation ends with a general conclusion on all work carried out in this thesis. We also presented some perspectives of future works on multichannel readout ASICs.

Chapter 1

LITERATURE REVIEW ON READOUT ASICs

1.1 Introduction

Radiation sensors detect and convert radiation into electric signals [1-4]. The study of signal processing chain is of a particular interest for understanding the characterization and working principle of many electronics devices encountered in various fields of science and technology such as telecommunication, medicine, high-energy physics and many more. This chapter provides a strong background on readout ASICs for radiation detection and solid-state detectors for X and Y rays spectroscopy and organised as follows: section 1.2 provides some generalities on ASICs for radiation detectors readout systems. In section 1.3, we present the architecture of general readout ASICs used in high-energy physics experiment, medicine and telecommunications. Radiation effects on ASICs chip is well discussed in section 1.4. Sections 1.5 and section 1.6 deals respectively with detectors technology and applications of ASICs chip in industry, medicine and high-energy physics experiments. The chapter is concluded in section 1.7.

1.2 Generalities on ASICs chip for radiation detectors readout systems

1.2.1 Definition of ASICs

Application specific integrated circuits (ASICs) refer to integrated circuits dedicated to specific purpose (application). ASIC design is a methodology of cost and size reduction of an

electronic circuit, product or system through miniaturization and integration of individual components and their functionality into a single element (ASIC) [1, 3, 4].An electronic product commonly consists of many integrated circuits (ICs) which are interconnected together to perform a particular function. For example, a 1980's smoke detector was built entirely of general-purpose ICs, such as amplifiers, comparators, regulators and discrete components such as resistors and capacitors [6, 7, and 8].It was expensive (component cost and assembly cost) and bulky (all those components required space). As competition intensified, the requirement for lower cost and smaller size drove the need for consolidation and integration of all those individual components into a single ASIC, reducing not only overall cost and size of the smoke detector but also improving its reliability (fewer parts, fewer things to go wrong). Recently, VLSI CMOS has played a crucial role in placing millions of transistors on a single chip, providing digital system designers with an ability to implement a vast number of gates with complex functionality on a single IC [5, 6]. Modern ASICs combine multiple complex blocks in a single package, including analog elements such as an amplifier, ADC, PLL and digital elements such as a microcontroller, ROM, EEPROM, RAM, and other building blocks. These types of ICs are known as system on chip (SoC) [7, 8]. The analog section of the ASIC is designed using primarily transistor-level design techniques and manual layout processes. The digital section of the chip is designed primarily using hardware description languages such as VHDL/Verilog followed by automated Place and Route (PnR) layout process. Since analog applications would typically involve higher voltages, such ICs would require their own unique set of manufacturing processes. In fact, a merger between analog and digital functionality onto a single silicon chip has increased market demands for a smaller size, lower power consumption, and higher speeds [7, 9, and 10].

1.2.2 Mixed-signal ASICs

The significance of mixed-signal integrated circuits is that it has both analog and digital circuits on just the same chip. Mixed-signal ASIC design offers engineers the potential to reduce complex, multiple-integrated circuit designs to a single IC [5, 6, and 9].

Mixed-signal ASICs also have become widely available and commercially viable. Some of the benefits of analog and mixed-signal ASIC are:

- Costreduction
- Improvedreliability
- Intellectualproperty protection
- Low power
- Miniaturization
- Performance improvement

Analog and mixed-signal ASIC design are both found in products used by millions of consumers the different segments of the market

- Healthcare to cosmetics
- Industrialsensors to flight control
- Instrumentation and measurements
- Mobile devices to credit card scanners

When building a mixed-signal ASIC design, you are combining the competences of the analog and digital circuit designs, which include:

- Analog-to-digital conversion via all methods, such as sigma-delta modulation
- Circuit design with linear circuits as well as switched capacitor circuit techniques
- Design of low power circuits
- Development of test procedures, test patterns, and test structures or ASICs
- Mixed-signal ASIC design and modeling

On the other hand, analog ASICs have played an important role in dayly live. In fact, the without the achievements of such technology, no portable electronic devices that we use in day-to-day life would seem to exist.We can just imagine a world without mobile phones, MP3 players, or navigation systems [8, 9, and 11]. Nevertheless, building these ICs on standard products would be expensive, as it is also impossible to bring them along with your pockets or purses.

Each automobile of today contains dozens of ASIC chips that enable the mechanism for climate control, deployment of the airbag, and suspension control to entertainment systems. At the same time, it can help many establishments, such as hospital/medical equipment, suspension control, and entertainment systems [2, 10,and 12].

1.3 Architecture of different detectors readout ASICs

1.3.1Analog signal processing chain

Traditionally, the electronic readout systems for the particle detectors have been made of almost all analog chains, as the one represented in Fig. 1.1 Each block of the chain has a specific function, so that you need to interconnect several blocks in order to make a system able to extract all the quantities of interest. With this approach, the A to D conversion is performed at the end of the acquisition chain, just before the readout interface connected to the computer [8, 9, and 11]. In most cases, the first stage of the chain is the preamplifierthat is usually located close to the detector. The preamplifier is a very low noise analog circuit that receives the weak signal generated by the detector and produces an output signal with an SNR ratio suitable for the transmission through a cable up to the readout electronics [10, 12]. The latter is normally housed in a crate or a rack and can be as far as ten or hundred meters from the detector. There are many types of preamplifier, but for the purpose of this document, we can consider them divided into two families: charge sensitive preamplifier and current sensitive preamplifier (or fast amplifier or wideband amplifier) [10, 11]. The charge sensitive preamplifier integrates the signal coming from the detector, thus it converts the charge into voltage amplitude. Ideally, it is just made of a simple capacitor; however, in order to avoid saturation, the integrating capacitor is put in parallel with a discharging resistor, so that the preamplifier output will have pulses with a fast rise time and an exponential decay (see Fig. 1.2). The charge information (energy) is here represented by the pulse height [11, 12].

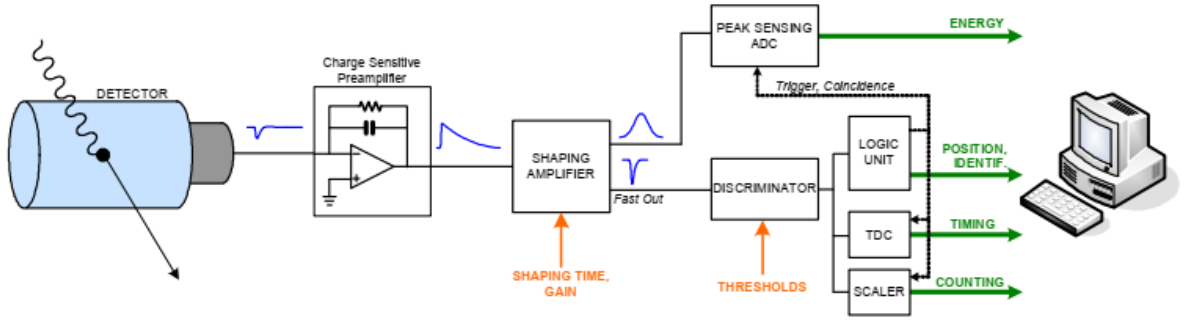


Figure 1.1: Block diagram of a traditional processing system for spectroscopy [12]

In order to preserve the timing information, the fast component of the signal (rising edge) is usually treated by a fast amplifier (or timing amplifier) that derivates the signal; the output of the timing amplifier usually feeds a chain made out of a discriminator, a time to digital

converter (TDC) and/or a scaler for the timing/counting acquisition. Further modules can be present in order to implement logic units, make coincidences (giving the position and the trajectory of the particles), generate triggers or give information about the pulse shape (time over threshold, zero crossing, etc) for the particle identification [2, 4, 5, 12]. Usually the fast amplifier is included in the shaping amplifier module and the relevant signal is provided as a separate fast output (or timing output).

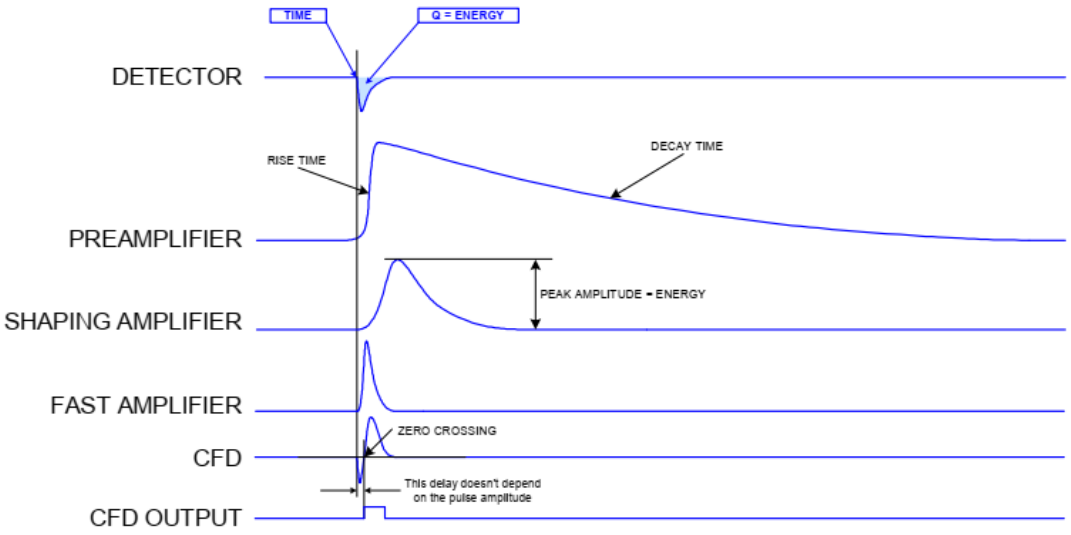


Figure. 1.2: Signal in the traditional analog processing chain [12]

Unlike the charge sensitive preamplifier, the current sensitive preamplifier is a linear fast amplifier that does not change the shape of the signal. Its output is normally a very short pulse (some tens of ns or even less) and is particularly used where the high precision timing information is an issue.

1.3.2 Digital signal processing chain: DPP strategy

With current analog pulse processing systems the preamp signal from the detector is shaped, filtered and amplified by a shaping amplifier, and then digitized by a peak sensing ADC at the very end of the analog signal processing chain. In digital pulse processing (DPP) systems, the detector signal form is digitized with a sampling (or digitized) ADC immediately after the preamplifier. The digitized signal pulse is then shaped digitally and the pulse height is extracted[10, 11, 12].

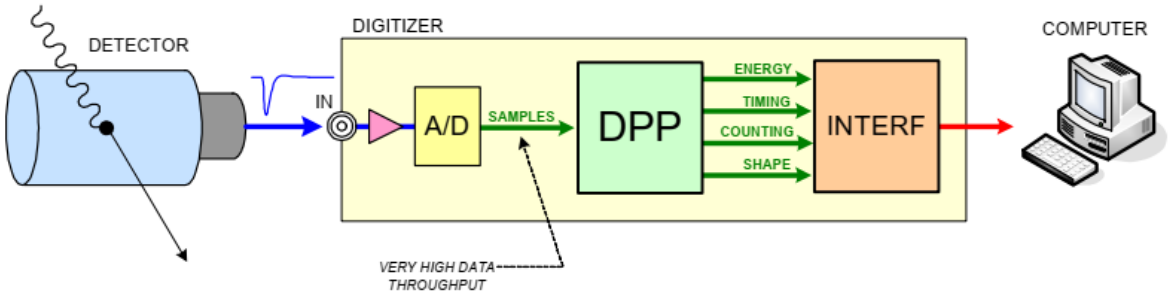


Figure 1.3: Block diagram of the digital pulse-processing unit for spectroscopy [12]

The digital processor is the key element doing this operation and either a field programmable gate array (FPGA) or a digital signal processor (DSP) can be employed. After extraction of the pulse height, one count is added to the memory address corresponding to the pulse height as in analog pulse processing [11, 13].

A DPP allows implementation of signal filtering functions that are not possible through traditional analog signal processing. Digital filter algorithms require considerably less overall processing time, so that the resolution remains constant over a large range of count rates whereas the resolution of analog systems typically degrades rather rapidly as the counting rate increases. As a result, the DPP will provide a much higher throughput without significant resolution degradation. Improved system stability is another potential benefit of DPP techniques. The detector signal is digitized much earlier in the signal processing chain, which minimizes the drift and instability associated with analog signal processing.

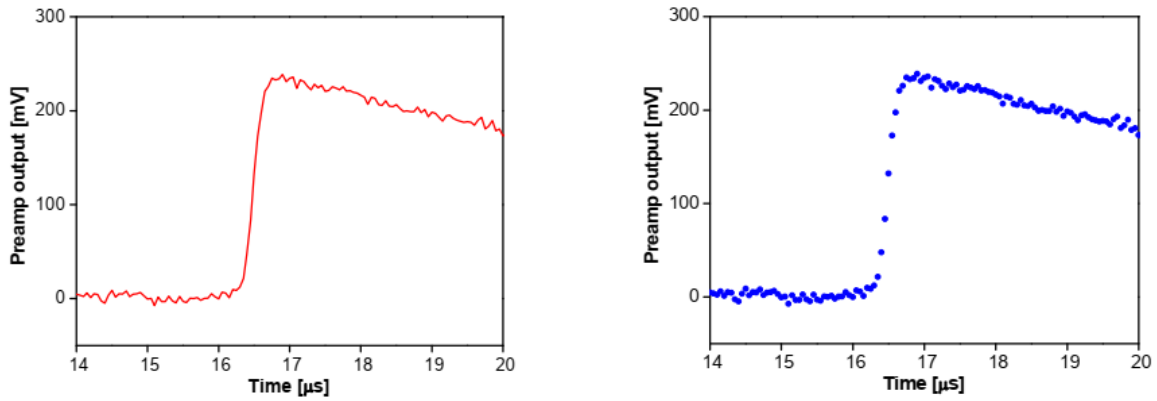


Figure 1.4: Signal pulse from a preamplifier and its digitized form [4, 13].

Figure 1.4 shows the output pulse of the preamplifier following a detection event and its digitized form. Since the signal has been digitized, it is no longer continuous. Instead, it is a

string of discrete values (Vin [1], Vin [2]… Vin [i],…). The first step is to apply an appropriate filter as in the analog pulse processing [11, 13].

1.4 Radiation Effects in front-end electronics

An ASIC chip is made of multi-channel front-end circuit, based on MOSFET devices. Therefore, radiation effect in ASIC is those created by charged particles in its front-end electronics.A typical CMOS transistor is shown in Fig.1.5. It is obtained from a silicon wafer with a sequence of steps (i.e. ion implantation, deposition of oxides, etching, annealing, etc.) widely described in [10, 12]. At the end of the fabrication process, a transistor is a device with four terminals: source, gate, drain and bulk. It becomes conductive device when it is proper biased. In particular, applying a positive voltage at the gate (respect to the source), a negative charged inversion layer appears connecting source and drain.This is a conduction channel with resistor feature [11, 13]. A current I_{DS} flows in the channel when at the drain there is a positive voltage respect to the source. The current is due to a flow of electrons from drain to source. The channel conductivity and the number of the electrons that reach the source depends on the speed acquired along the channel, on the gate and bulk voltages, on the Cox and C_D channel capacitances. The I_{DS} current starts flowing as soon as the overdrive voltage becomes positive. It is defined as the difference between V_{GS} and V_{TH} (Threshold Voltage) voltages. The trend of the I_{DS} curve depends on the number of free carriers along the channel, which is directly related to V_{DS} and V_{GS}-V_{TH} voltages. For small V_{DS}, the channel appears homogenous with a resistor behaviour ($I_{DS}= V_{DS}/R_{DS}$). Increasing V_{DS}, the current assuming a parabolic trend up to reach a saturation value. Linear region is the first one; saturation region is the last one. Each region is characterized by a channel resistor R_{DS} given by (1) as follows:

$$R_{DS} = \rho \frac{W}{t_{ox}} = \frac{1}{nq\mu_n} \frac{W}{t_{ox}} \quad (1)$$

Where ρ is the resistivity of the channel, t_{ox} is the MOS oxide thickness, and μ_n is the mobility coefficient of the electrons near the silicon surface below the oxide layer, n is the number of the free carriers (electrons) resulting from doped silicon, and free to move along the channel. Considering the small signal model of a transistor, a small signal input voltage (V_{GS}) application produces a transconductance g_m given by (2).

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \quad (2)$$

All transistor features depend on flow of free carriers in the channel and their number. They could change in radiation environment. The main effect related to these phenomena is a

reduction of minority charges lifetime. Ionizing particles generate electron-hole pairs the inside oxides [14, 15, 16] that could disappear in the gate and the substrate for quantum tunnelling or remain in the oxides under the influence of the electrical field. The electrons, highly movable charges, are easily swept out from the oxide whereas the holes, being slower, move towards the SiO_2-Si interface. Some of these holes can be trapped in the lattice imperfections, originating this way a fixed positive charge in the oxide. Another effect of the ionizing radiation is the creation of the traps at the SiO_2-Si interface [15, 16]. The probability of having trapped positive charge in the oxide next to the silicon interface depends directly on the number of defects in the oxide. Trapped holes inside oxides and the interface traps generation affect the transistor electrical parameters.Semiconductor devices are subject to three radiation-induced effects [16, 17]: single event effects (SEEs), total ionizing dose (TID) and displacement damage (DD).

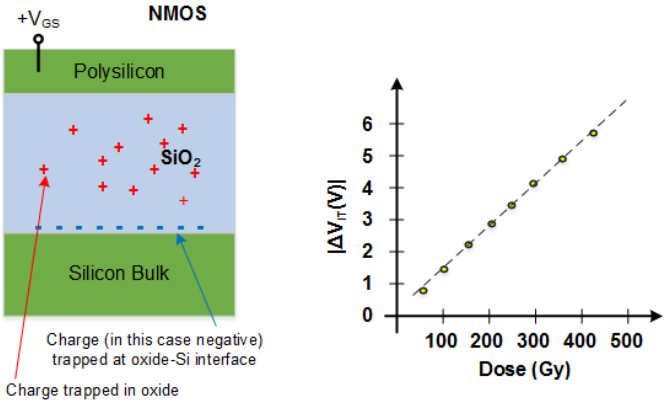


Figure 1.5: Threshold Voltage Shift due to Radiation [14].

1.4.1 Single Event Effects

As the density and functionality increases and power decreases, electronics sensitivity to radiation increases dramatically. There are different types of radiation damage in semiconductor devices varying from data disruptions to permanent damage. Single event effects(SEE) are device failures induced by a single radiation event [1, 18]. When a radiation event causes enough of a charge disturbance to reverse or flip the data state of a memory cell, the event caused is called Upset (Single Even upset). The device is not permanently damaged by the radiation, if new data is written to the bit it will stored correctly [1, 3, 19]. However, an unintentional short circuit between components on an integrated circuit can create a Single Event Latch up (SEL) [1, 18 and 20].

1.4.2 Total Ionizing Dose Effects on MOS Transistors and Integrated Circuits

The Radiation-Induced Narrow Channel Effects (RINCEs) is linked to the Shallow Trench Isolation (STI) oxide present in modern devices. The STI encloses the transistor in order to avoid leakagepaths between adjacent devices in integrated circuits but its important thickness presentsone of the weaknesses of modern technology against TID. Indeed, the scaling of the CMOS technology concerns mainly the gate oxide and the STI thickness is not reduced accordingly [1, 20]. Fig.1.6 illustrates the STI surrounding an n-channel MOSFET before (top) and afterirradiation (bottom) for a narrow (left) and wide transistor (right). Before irradiation, the STI facing the channel contains a negligible amount of charges and the current simply flows through the channel without any influence. During and after irradiation, the accumulation of oxide and interface traps occurred and charges begin to accumulate in the area facing the channel. The trapped charges create an electric field that affects the current flowing through the transistor channel. The width *W* of the transistor plays a key role in this effect. As shown in Fig.1.6, the smaller the *W*, the larger the part of the channel impacted by the generated electric field [16, 19, 20].

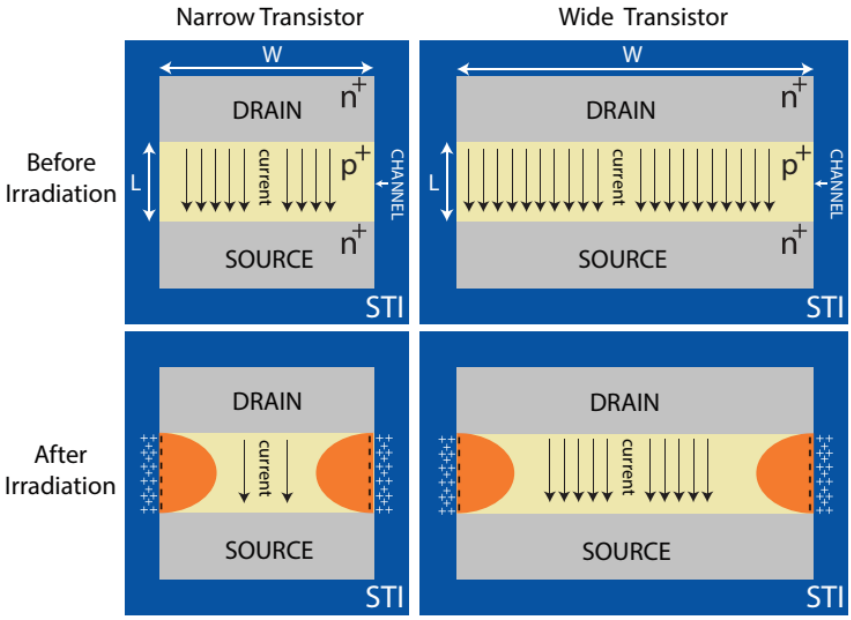
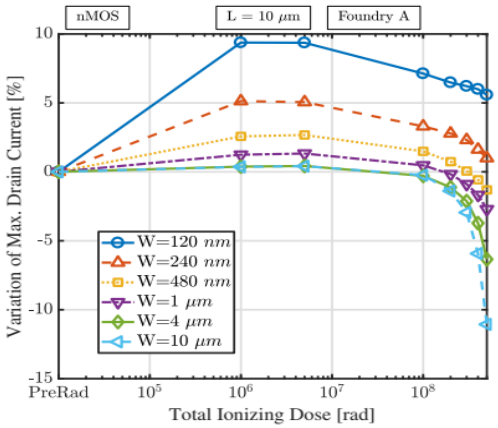
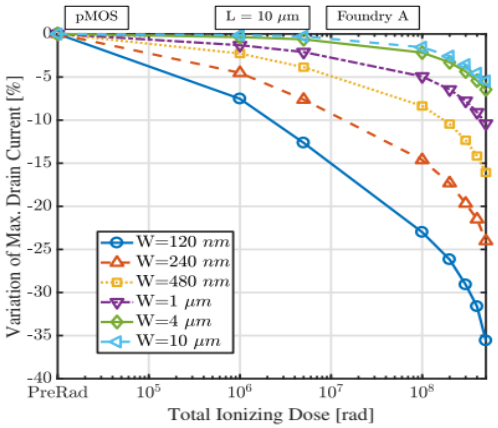


Figure.1.6: *Radiation-Induced Narrow Channel Effect related to the presence of the Shallow Trench Isolation. The top left and right n-channel MOSFETs are non-irradiated with two different widths while the two bottoms left and right n-channel are irradiated. The charges build up at and near the Si/SiO$_2$ interface (oxide traps and interface traps) [20].*

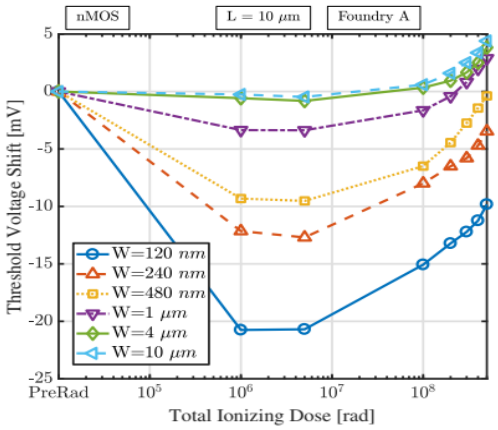
The channel width dependence is outlined in Figure 1.7 where the maximum draincurrent and threshold voltage shift features are extracted from the $I_D - V_G$ characteristicof transistors irradiated up to 500 Mrad at room temperature [17, 20]. The channel width *W* ofthe transistors varies from 120 nm to 10 µm and the channel length *L* is fixed at 10 µm,since, as we will see later, the effects associated with spacers (RINCEs) are less importantwith greater channel length. The consequences of this charge build-up are different for n-channel and p-channel MOSFETs. The generation of oxide traps is faster than interface traps and therefore inn-channel MOSFETs, where oxide and interface-trapped charges are opposite in sign, two different trends are observed. First, the accumulation of positive trapped charges in the STIproduces a negative threshold voltage shift of the transistors (Fig.1.7c) and, therefore, anincrease in the maximum drain current (Fig.1.7a) with a peak around 1 Mrad [20, 21]. Second, the slower build-up of interface traps gives rise to the so-called rebound in the evolution ofthe electrical parameters: an increase in the threshold voltage and hence, a decrease in the maximum drains current. For p-channel MOSFETs, interface traps carry a positive charge and thus both oxide and interface traps are positively charged. The maximum drain currentand the threshold voltage are both monotonically decreasing during irradiation (Fig.1.7b and Fig.1.7d). We can observe that in both n- and p-channel MOSFETs the threshold voltageshift and the maximum drain current variation are inversely proportional to the width of the transistor [18, 19, and 20].



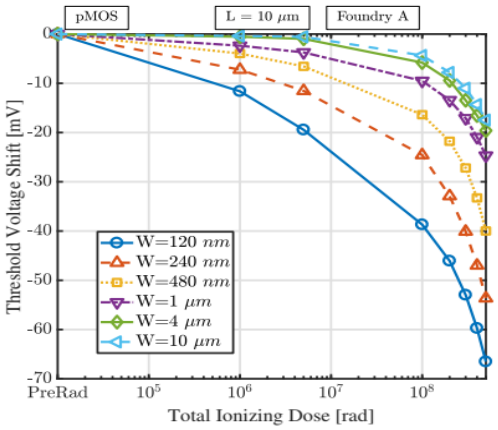
(a) Maximum drain current variation in n-channel MOSFETs



(b) Maximum drain current variation in p-channel MOSFETs



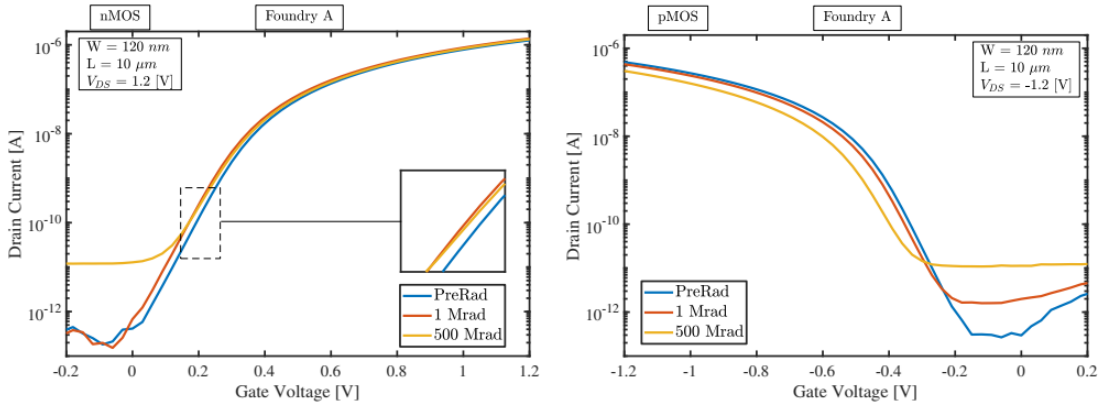
(c) Threshold voltage shift in n-channel MOSFETs



(d) Threshold voltage shift in p-channel MOSFETs

Figure 1.7: *Variation in the maximum drain current in saturation ($|V_{DS}|$= 1.2 V) and threshold voltage shift for n-channel MOSFETs (a and c) and p-channel MOSFETs (b and d) during irradiation up to* 500 Mrad at 25° C. *The variation is strongly dependent on the channel width. The channel length of the transistor is fixed and very large to mitigate the spacer-related effects. The transistors were biased during irradiation in diode configuration ($|V_{DS}|$= 1.2 V and $|V_{GS}|$= 1.2 V) [20].*

The $I_D - V_G$characteristics of the narrowest n- and p-channel MOSFETs transistors are respectively shown in Fig.1.8a and 1.8b. For the n-channel MOSFET, we can observe between 1 Mrad and 500 Mrad the increase in the subthreshold swing related tothe build-up of interface traps (zoom in Fig.1.8a) [19, 20, 22].

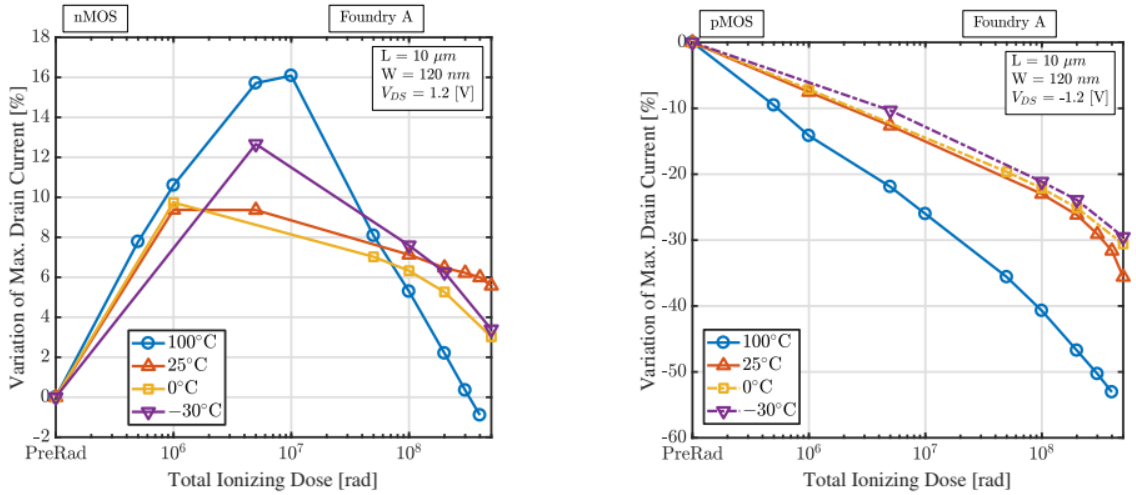


(a) n-channel MOSFET *(b) p-channel MOSFET*

Figure 1.8: I_D - V_G *characteristics before irradiation, after* 1 Mrad *and* 500 Mrad [20]

Irradiations at different temperature have been performed from -30 ◦C to 100 ◦C (Fig.1.9). In n-channel MOSFETs, the influence of temperature is difficult to interpret. Indeed, holes trapping process is enhanced at low temperature but the transport of both holes andprotons near the interface Si/SiO_2 is slowed down and thus the observed degradation isdifficult to interpret. We can conclude that temperature increases the magnitude of thechange as we observed sharpest variation at 100^o C. The interpretation for the p-channel MOSFETs is straightforward as both mechanisms are participating to the degradation: higher temperature leads to a higher degradation [21, 22].

A comparison is performed between foundry A and B (Fig.1.10). The increase in the maximum drain current due to radiation induced narrow effect is happening at the same range of TID in both foundries and is due to the same threshold voltage shift but the magnitude is more important in foundry B. This difference can be explained by the fact that more oxygen vacancies are present close to the interface and therefore more oxide traps are accumulated in the region close to the channel of the transistors [20, 22]. Nevertheless, the impact of the interface traps is similar in both foundries. For the narrowest transistor, we can observe a decrease of 2 % just after the peak. For PMOS transistors similar degradation is observed in both foundries. Foundry C is left out from the comparison due to the lack of adequate transistor dimensions but has shown qualitatively similar dependence [20].



(a) n-channel MOSFET *(b) p-channel MOSFET*

Figure 1.9: *Influence of the temperature on the Radiation-Induced Narrow Channel Effect (RINCE) in n- and p-channel MOSFETs [20].*

The electric field applied to the transistor during irradiation has a major influence on the behavior of the device because it is responsible for the drift of charges in oxides Fig.1.11 presents the influence of the polarization of the RINCEs in a narrow and long device NMOS and PMOS transistors have been kept under bias during irradiation with different bias possibilities for drain and gate [19, 20, 22]. In PMOS transistor (Fig.1.11b), the degradation is higher when the gate bias is applied, no matter the applied bias of the drain. The difference observed between the two degradations is due to a further increase of the threshold voltage due to oxide traps because no major change in the subthreshold swing is observed between the different configurations (not shown). The effect of polarization is more important and complex in the NMOS transistor (Fig.1.11a). The first increase in maximum drain current at 1 Mrad due to oxide traps is not dependent on bias but the behaviour after 10 Mrad is strongly bias dependent and both gate and drain bias influence the evolution. After 10 Mrad, the presence of the gate bias induces a decrease of the maximum drain current due to the accumulation of interface traps observed by the increase of the subthreshold swing (with andwithout drain voltage) [22].

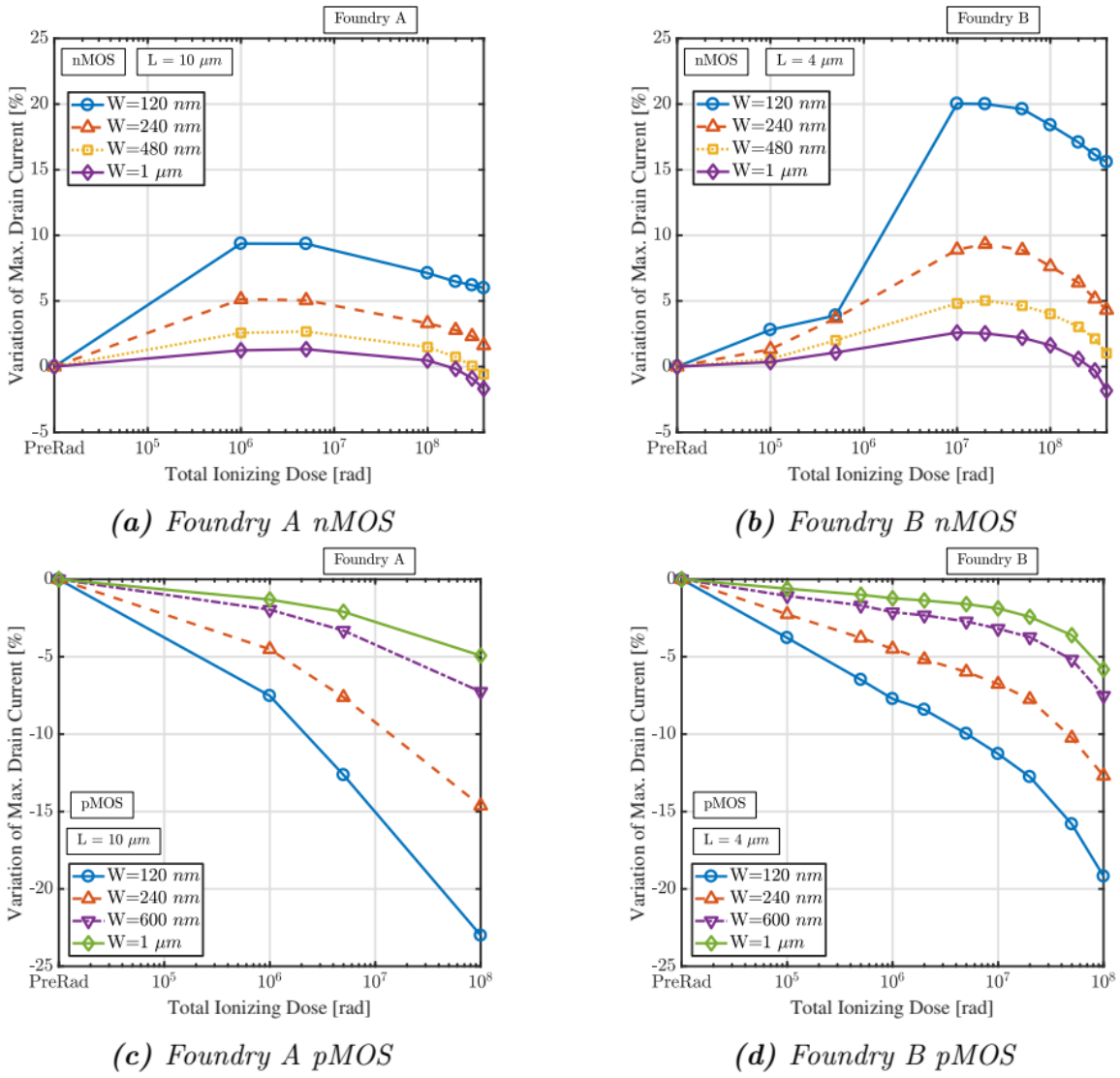
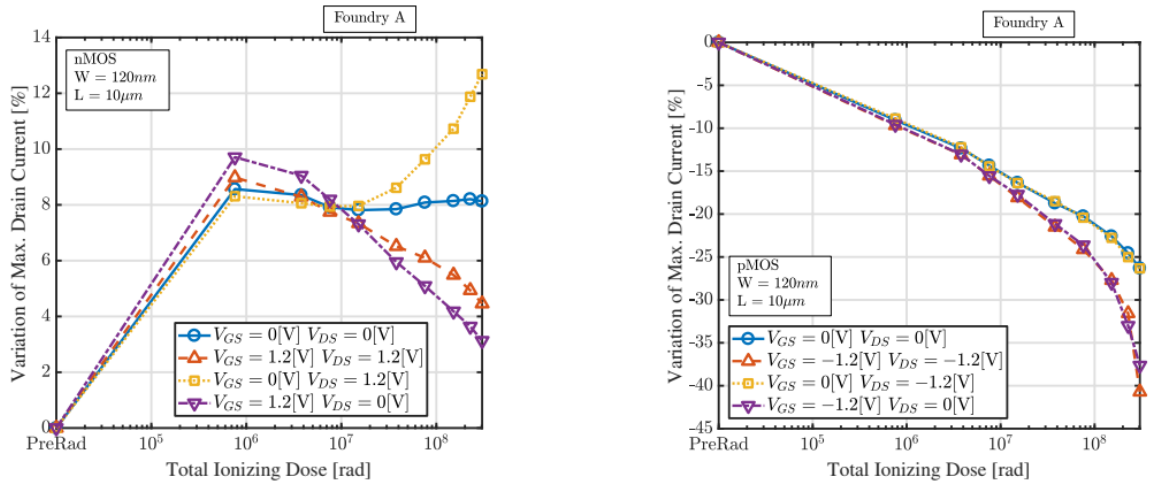


Figure 1.10: Radiation-Induced Narrow Channel Effects (RINCEs) for two different foundries with transistors of the same channel width and a large fixed channel length to alleviate the effects of the spacers [20].

Without gate bias, there is no build-up of interface traps and two different trends are observed. First, if no bias is applied at all (both gate and drain are at 0 V), we observednosignificant change in the transistor characteristic up to 300 Mrad. However, when drainbias is applied, a second accumulation of oxide traps is observed, leading to a second increase in maximum drain current. This second increase is mainly due to an increase in transistor transconductance, which means that an increase in gate voltage induces a higher current than before. To the best of our knowledge, this behaviour has not yet been observed [20, 21].



(a) n-channel MOSFET *(b) p-channel MOSFET*

Figure 1.11: *Influence of the transistor bias during irradiation for RINCEs [20].*

Threshold Voltage Shift in Transistors

Positive charged trapped in the oxide (Δ*Vox*) and interface traps (Δ*Vit*) appear after irradiation. For this reason, flat-band voltage changes shifting the threshold voltage with an amount of voltage given by (3) [18, 21].

$$\Delta V_{ox} = -\frac{1}{C_{ox}} \int_0^{t_{ox}} \frac{x}{t_{ox}} \rho(x) dx \quad (3)$$

Where$t_{ox}$is the thickness of the gate oxide, C_{ox} is the capacitance per unit area and ρ(x) is the charge distribution in the oxide per unit volume, as function of the distance from the gate-oxide interface (x). From (3) results that the voltage shift is negative when the trapped charges are positive. The presence of interface traps, instead, causes a positive (Δ*Vit*) shift according to (4) and figure.

$$\Delta V_{IT} = -\frac{\Delta Q_{IT}}{C_{ox}} \quad (4)$$

Where Δ*Qit* is the charge difference, per unit area, which fills the interface states before and then the irradiation. In NMOS transistor, interface state creation is a slower phenomenon that causes an initial threshold voltage reduction followed by a definitively increase. It's worth to be said that, especially in more scaled technologies, the thinner gate oxide makes the radiation-induced charge contribution negligible if compared with the effects of the interface states. For this reasons the NMOS transistor threshold voltage tends to increase in any case [1,2, 20, 21, 22, 23].

Transconductance or Gain of the Transistors

The transconductance of the MOS transistor is decreased by radiation-induced reduction in carrier mobility in the device channel caused by charges trapped at the silicon/silicon dioxide interface. Transconductance can also be decreased by increases in surface resistivity [5, 22 - 29].

Leakage Current

Leakage current may be generated or worsened with charges trapped in the oxides. This effect depends on Shallow Trench Isolation (STI) oxide and its thickness. This effect can only appear in the n-channel MOSFETs because the positive oxide traps accumulated in the portion of the STI facing the channel can locally attract electrons from the p-substrate and thus create a parasitic conductive path between source and drain (Fig.1.12(1)). Charges in the STI can also create a leakage path between two n-doped regions of different potential creating parasitic leakage currentbetween adjacent devices (Fig.1.12(2)) [23, 24, 26].

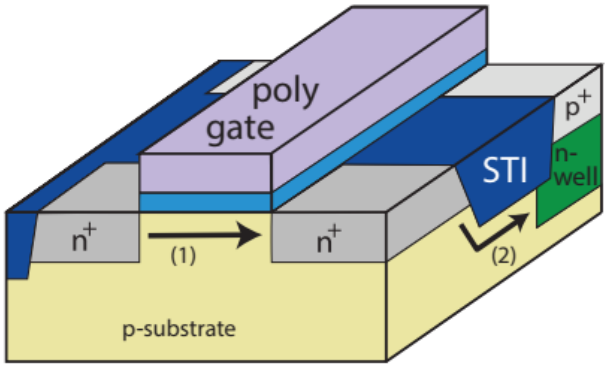


Figure 1.12: Cross-section of an n-channel and p-channel MOSFETs. The build-up of oxide traps in the STI can create a parasitic path between the source and the drain in n-channel MOSFET (1) and between two n-doped silicon regions of different potential (2) [26].

In the history of studying the total ionizing dose effects in transistors, the increase of the leakage current has been the major threat to the use of commercial technologies in radioactive environment [23, 24, 25and 26]. The most commonly used technique to eliminate leakage current between sources and drain (Fig.1.13 left) is the enclosed layout transistor (Fig.1.13 right). Indeed, in enclosed transistors, the STI does not face the channel. The enclosed layout transistor as a HBD technique was used in the electronics developed for the Large Hadron Collider to eliminate the leakage current present in the 0.25µm technology used at that time

[25, 26, 27]. However, this type of transistor requires a considerable effort to be characterized and presents several drawbacks compared to standard layout transistor (e.g. largerdimensions, asymmetric, increased parasitic capacitance) [28, 29].

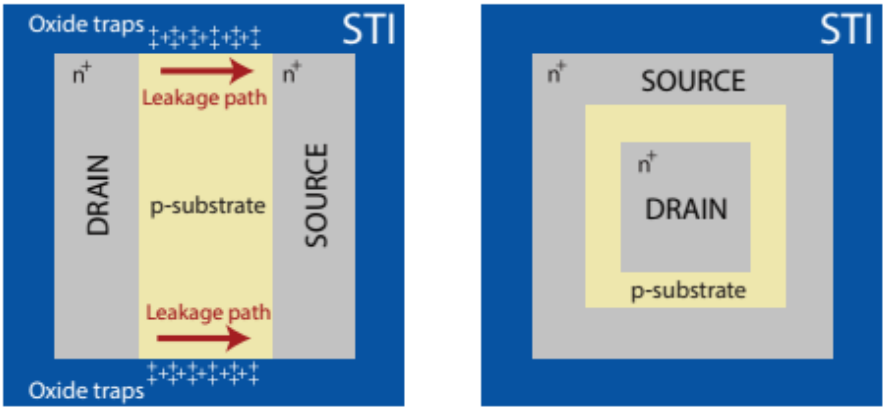


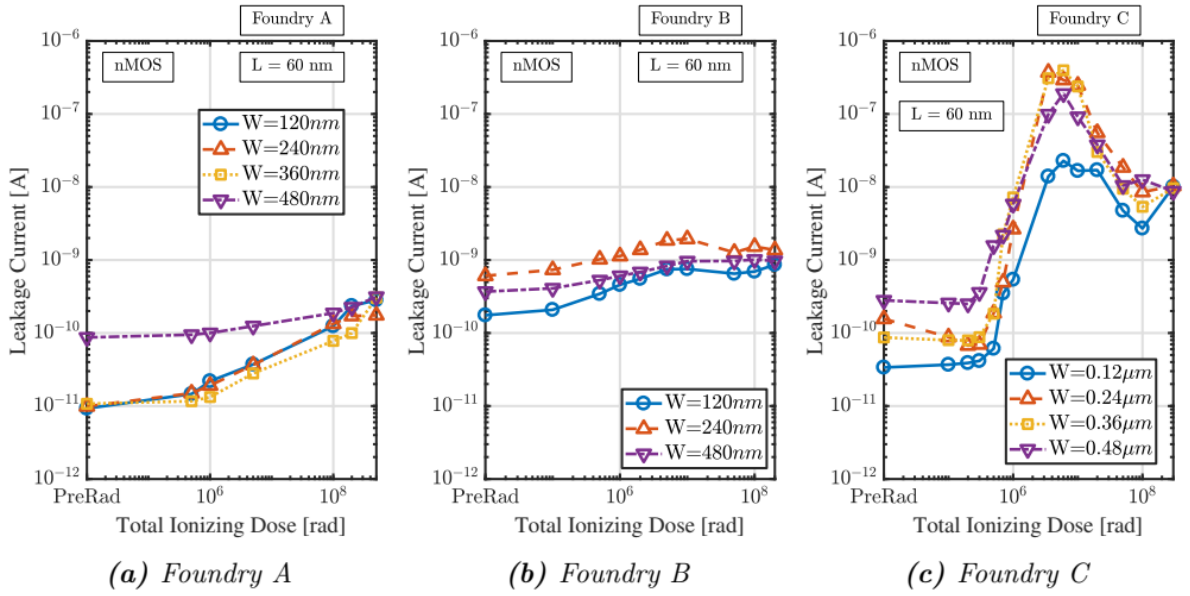
Figure 1.13b: *Standard layout transistor (left) can present leakage current. Enclosed layout transistor (right) is a hardening-by-design (HBD) technique that eliminate the impact of the Shallow Trench Isolation (STI) [30].*

In the 65 nm technology used (foundry A), the radiation-induced increases if the leakage current observed is negligible even at very high total ionizing dose (TID) (Fig.1.14) and therefore the use of enclosed layout transistor can be avoided. Foundry B presents also a negligible variation of the leakage current (Fig.1.14b) but foundry C has an important increase by 3orders of magnitude (Fig.1.14c). This strong foundry-to-foundry variation can be ascribed to the fabrication processes of the STI [20, 30, 31] as it has already been observed in 130 nm technology [32, 33, 34] but also maybe to the difference in the doping profile of the transistors.

Pulse Rise Time

Many detectors are operated with electric fields high enough to result in saturated drift velocities to make the collection of charge carriers fast. This way, rise time of the signal pulse will roughly be under 10 ns for typical detectors. The total detector contribution to the rise time is composed of charge transit time and plasma time [8, 29, and 30]. Charge transit time is the time for migration of electrons and holes formed by the incident radiation across the region of high electric field in the depletion region. In much depleted detectors, the depletion width is fixed by the physical thickness of the silicon wafer and therefore the transit time is

decreased when the bias voltage is increased [4, 8, 20, 23]. Plasma time is observed when the radiation is heavy charged particles. The density of the electron hole pairs is then enough to form plasma-like cloud of charge that shields the interior from the electric charge. The plasma time is defined as the time required for the cloud to disperse and normal charge collection to begin [4, 17, and 29]. The dominant advantage of semiconductor detectors over gas-filled detectors is the amount of ionization energy required to create an electron-hole pair, which is 3.6 eV for silicon compared to about 30 eV for gas.



(a) Foundry A *(b) Foundry B* *(c) Foundry C*

Figure 1.14: *Evolution of the leakage current in n-channel MOSFETs in foundry A, B and C. Foundry C has an important increase of the leakage current (3 orders of magnitude) while foundry A and B present a negligible increase [30].*

Because of this, the statistical fluctuation in the number of carriers per pulse becomes a smaller fraction of the total and the greater amount of charge per pulse leads to a better signal to noise ratio [4, 20, 29, and 31].

1.5 Detector Technology

1.5.1 Materials for Semiconductor Detectors

A good material for a solid-state detector should possess the following features:

- large signal in response to particle/photon deposited energy, which requiresa small energy bandgap of a given material to ensure low average energy for the hole-electron generation.

- low atomic number Z and low density in case of tracking application for particlephysic experiments (particle energy is measured in the calorimeter system).
- high atomic number Z and high density in case of X-ray and γ-ray spectroscopic and imaging applications; high density leads to a large energy loss per traversed length and higher probability of absorbing all photons in a beam.
- high mobility of charge carriers and no trapping effects to collect all the generated charge in a short period of time (important for an operation with high radiation intensity).
- large carrier lifetime to increase so-called charge collection efficiency, defined as a collected charge on the electrode to a total deposited charge.
- low leakage current in room temperature; too small bandgap can result in a significant thermally generated current.
- large and high quality crystal (good homogeneity, low impurity levels, high resistivity) to produce a large area detector.
- radiation hardness especially in case of new accelerator experiments where radiation doses are really high.
- stable and matured industrial fabrication and processing with relatively low cost and good availability.

Table.1.1shows the main parameters of different semiconductor materials and diamond (insulator) often used to produce Position Sensitive Detector (PSD).

Table.1.1: Important parameters of materials used for semiconductor detectors

Parameters	Si	Ge	GaAs	CdTe	CdZnTe	Diamond
Average Z	14	32	31/33	48/52	48/30/52	6
Energy bandgap (eV)	1.12	0.67	1.43	1.44	~1.6	5.48
Density(g/cm^{-3})	2.3	5.3	5.4	6.1	5.8	3.5
Energy of electron-hole pair generation (eV)	3.64	2.96	4.2	4.43	~4.6	13.1
Mobility at T=300K(cm^2/Vs)	1350	1900	8000	1100	~ 1000	1800
- Electrons	480	3900	400	100	~ 100	1200
- holes						
Carrier lifetime (μs)	~250	250	10^{-3}- 10^{-2}	~10^{-1}-2	~10^{-1}-2	10^{-3}

For nearly three decades, **silicon** has been the most popular material used for semiconductor detectors [23, 29 and 37]. A very advanced silicon technology is driven by electronics industry. The silicon material fulfils nearly all of the above points, with the exception of high *Z* and radiation hardness. Because of low *Z* =14 and matured stable technology, it is very attractive for a tracking detector in particle physics experiments. These experiments are often performed on high luminosity machines like the Large Hadron Collider (LHC), where the expected radiation doses are very high. For silicon tracker doses up to 10 Mrad of ionizing particles and fluencies of 10^{13}-10^{14} neutron/cm^2 are expected in over ten years of LHC operation [20, 37 and 38]. In such conditions, both the bulk damages [39, 40] and ionization effects in silicon oxide [41, 42] are observed. The low *Z* and low silicon density limit its X-ray applications mainly to low energy photons. A standard 300 μm thick detector converts nearly all 8 keV X ray, but only ∼26.7% of20 keV X-ray and ∼2% of 60 keV X-ray. Therefore, many laboratories make an effort to produce detectors more efficient for high X-ray energy, with the use of other semiconductor materials [43, 44.], such as high purity germanium (Ge) and compound semiconductors, like gallium arsenide (GaAs), cadmium telluride (CdTe), cadmium zinc telluride (CdZnTe).

. Germanium has smaller bandgap than silicon (0.67eV vs. 1.12eV for Si) and has a very good energy resolution [43, 45 and 46]. However, low energy bandgap greatly increases a reverse current and a Ge detector typically is cooled to nitrogen temperature (77 K). Germanium, because of high photo-absorption cross section σ*photo* ∼*Z* 4-5, is more attractive for higher X-ray energies than silicon [42, 46].

. Gallium arsenide has been studied as the material for a semiconductor detector for γ-ray since the early 1960's [43, 44 and 47]. Because of its potential radiation hardness, it is also used in military applications and tested for possible applications in particle physics experiments. GaAs has relatively high mobility. Because of impurities in the order of 1015cm^{-3}, its carrier lifetime is only 10 ns. Due to trapping effects, it also suffers from an incomplete charge collection.

. CdTe and CdZnTehave high density and high *Z* (*ZCd*= 48, *ZTe*= 52, *ZZn* =30). Because of large photon absorption cross section and possibility of operation at room temperature, they are used for X-ray and γ-ray spectroscopic and for medical imaging applications [48, 49, and 50]. CdTe and CdZnTe generally suffer from poor hole collection. The hole mobility is very low μ*h* ≈ 100 cm^2/Vs and tends to be much smaller than for electrons μ*e* ≈ 1000 cm^2/Vs.

The detectors with CdTe Schottky contacts have lower leakage currents than ohmic devices. However, Schottky detectors have a problem with polarization effects [17, 51]. The technology of CdTe and CdZnTe detectors is still limited to small crystal and the connections with front-end electronics are more difficult than in case of Si detectors.

. Diamond, as a material with low *Z,* is a good candidate for tracking applications in particle physics [8, 17, and 52]. It has very good radiation hardness, even for radiation expected at LHC. Diamond is classified as an insulator and in order to create hole-electron pair, an average energy of 13.1 eV is required. Large detector samples have not been achieved yet. Because of very long trapping times, the signal from a diamond detector increases during radiation ("pumping" or "priming" effect [4, 17 and 53].

1.5.2 Silicon Diode Detectors

Silicon diodes have become the most popular type of detectors for detection of heavy charged particles. They are often used for alpha particle and fission fragment spectrographs. The advantages of silicon detectors are [4, 8, 10 and 11]:

• good energy resolution
• good stability
• excellent timing characteristics
• very thin entrance window
• simplicity of operation

P-N Junction and Reverse Biasing

The junction of p-doped and n-doped silicon, generally known as a diode configuration, has many favourable properties. The concentration of electrons is much higher in n-type region. The discontinuity in electron density causes a net diffusion from regions of high concentration to lower concentration regions [4, 8, and 10]. This causes a net negative space charge in the p-region and a net positive space charge on the n-region. This region is called the depletion region and it extends to both n- and p-region. When a reverse bias is applied to the region, virtually all the applied voltage will appear across the depletion region, since its resistivity is much higher than that of a normal n- and p-type material. Reverse biasing also increases the size of the depletion region because of the accentuated difference across the junction. The diode detectors are therefore biased with the largest possible voltage so that the

detector is fully depleted but under the breakdown voltage, which could destroy the semiconductor detector [4, 8, and 20].

Silicon PIN Detector

In this detector configuration, a high-resistivity i-region is provided with p and n non-injecting contacts at either surface to help reduce the leakage current to below that which would be observed with a simple diode. A typical thickness of 300 μm is sufficient to provide useful detection efficiency up to 20 or 30 keV [8, 17 and 20].

Silicon Drift Detectors (SDD)

The basic working principle of the SDDs is similar to that of a simple PIN diode detector for radiation detection [54, 55, 56, and 57]: to develop a region within the devicedepleted of all free charge carriers so that any electron-hole pairs generated by an ionizing radiation can be readily separated. Both of these effects are normally achieved by reverse biasing the PIN diode and this can be seen in Fig.1.15 (a). On the left side of Fig.1.15 (a), a plot of the voltage potentialas a function of depth is also shown. Here, it can be seen that most of the N-type substrate is at same potential and hence any e-/hole pairs generated here cannot be separated from each other.However, it is possible to grow a wafer with two p+ electrodes on both sides of the device with a very small n+ electrode on one side as shown inFig.1.15 (b) [4, 8, 11]. A quick look at the plot of voltage potential as a functionof depth for Fig.1.15 (b) shows that now there are two different regionswhere the detector has been depleted. Now if we keep on increasing the positive biasing voltage V*biasc* at the n+ electrode, a moment comes when the whol region between the two p+ electrodes is depleted. This voltage which completely depletes the silicon wafer is known as the *depletion voltage* V*dep* and is nominally four times lower than the voltage needed to deplete the PN diode of similar thickness [4, 10, 54 and 55]. This last scenario is shown in Fig.1.15(c) where the minimum potential across the depletion region lies between the two p+ electrodes. The Silicon Drift *Detector* works on the sideward depletion principle described for a PIN diode in Fig.1.15 [4, 8, 54, and 55].

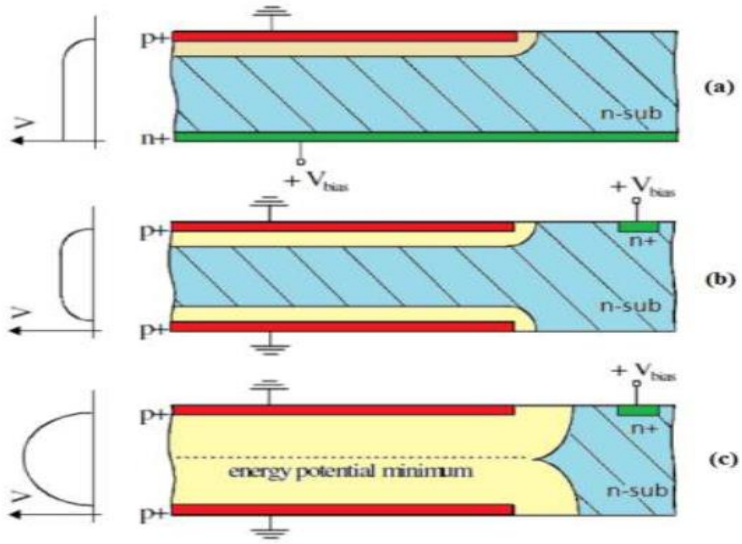


Figure 1.15: *(a) Depletion of a PIN diode. (b) Partial and (c) full side-ward depletion in a modified PIN diode [54, 55].*

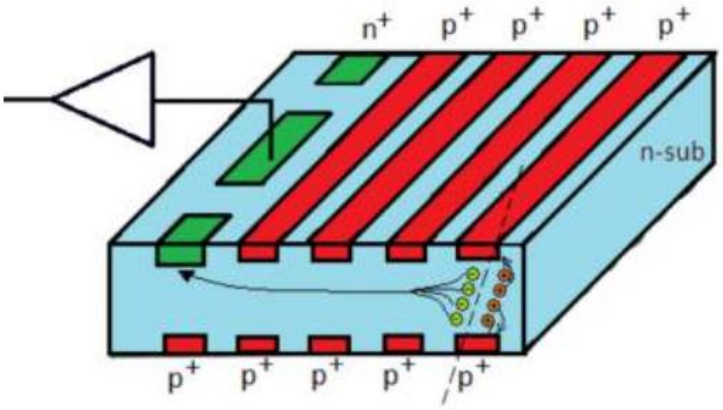


Figure 1.16: *SDD working principle: e-/hole pairs generated by ionizing radiation within the depletion region are separated by the electric field [54, 55].*

However, in case of the Silicon drift detectors an additional electric field is added parallel to the surface of the wafer so that the drifting electrons can be forced to move towards the n+ electrode. This is achieved by introducing two arrays of p +electrodes on both sides of the wafer as shown in Fig.1.16 as compared to single large p+ electrodes (Fig.1.15). These p+ electrode arrays are suitably biased to create an additional potential gradient in the direction of n+ electrode and toward the surface [54 - 57].

Silicon pixel-strip sensors.

The operating principle of a pixel-strip sensor is illustrated in Fig.1.17 [57]. To readout, the sensor's hits and locally process and compress higher particles flux, the readout electronics of the short strip ASIC are needed to be implemented within a CMOS process and integrated into the sensor's chip; this will avoid loss of transmission between the high-speed interconnects and the readout ASIC chip.

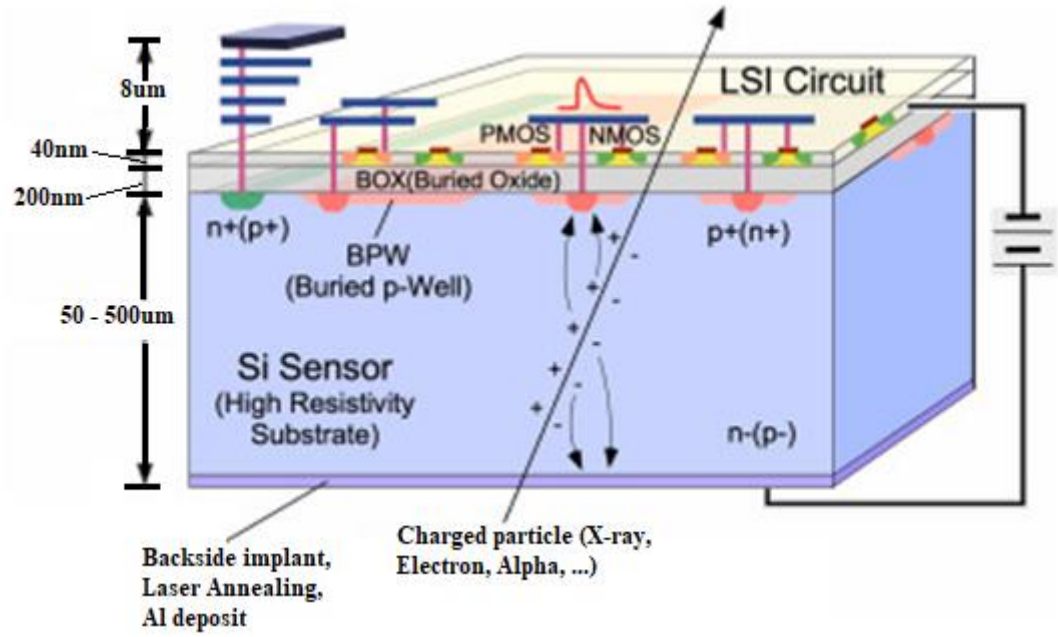


Figure.1.17. Principle of operation of a silicon pixel-strip sensor [57].

1.5.3 Scintillation Detectors

Scintillation is the process of producing light. Scintillation radiation detectors convert light to an electrical pulse. Although scintillation is one of the oldest techniques for radiation detection, many modern detectors exist that use this principle. There are different types of scintillating materials, the most important being:

- Organic Scintillators
- Inorganic Scintillators
- Unactivated and Activated Fast Inorganics
- Transparent Ceramic Scintillators
- Glass Scintillators
- Noble Gas Scintillators

The scintillation process works by converting a small fraction of the kinetic energy lost by a particle in a scintillator into fluorescent energy. The fraction of the energy converted depends on both the type of particle and its energy. Because of the dependence of the type of particle, the absolute light yield of a scintillator is described by MeV electron equivalent (MeVee). The energy required to generate 1 MeVee is 1 MeV for fast electrons but can be several electron volts for heavy charged particles [8, 17 and 57].

1.6 Applications of readout ASICs chip in medicine and high-energy physics area

1.6.1 Applications in medicine

Microelectronic recording interfaces are widely used in neuroscience research as well as in diagnostic and therapeutic technologies. The high-quality amplification of weak neural signals remains a challenge in both data acquisition and diagnostic devices. Important examples of neural recordings include electrocorticograms (ECoG) [56, 58] and electroneurograms [58, 59]. In addition, neural recordings are essential for brain–machine interfaces and closed-loop therapeutic devices that interface with the brain, nerves or visceral organs [58 - 60]. The key requirements in the above applications are to acquire, amplify and process neural signals using low-noise amplifiers and associated signal conditioning circuits [61]. The amplified and processed recordings may then be used in research, clinical diagnostics or, in the case of closed-loop therapeutic devices, functional electrical stimulation.

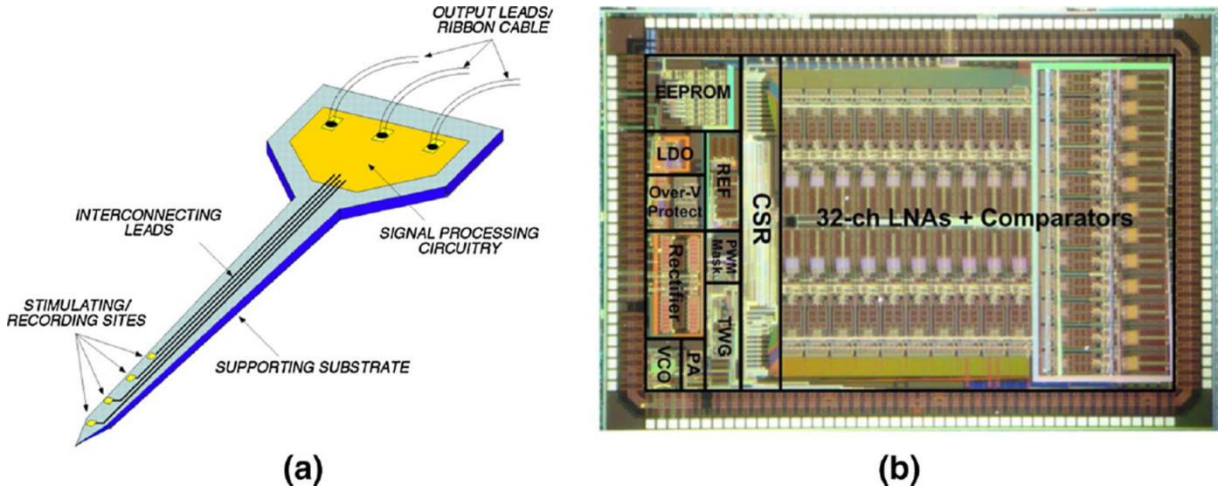


Fig.1.18: (a) *Early manifestation of a complete neural recording amplifier system proposed by Wise and Najafi [62].* ***(b)****A recent state-of-the-art implementation of a neural amplifier system reported by Lee et al. [63]. Measuring 4.9 mm by 3 mm, neural amplifiers, analog-to-digital converters, inductive power harvesting and a digital data transmitter are included on a single chip.*

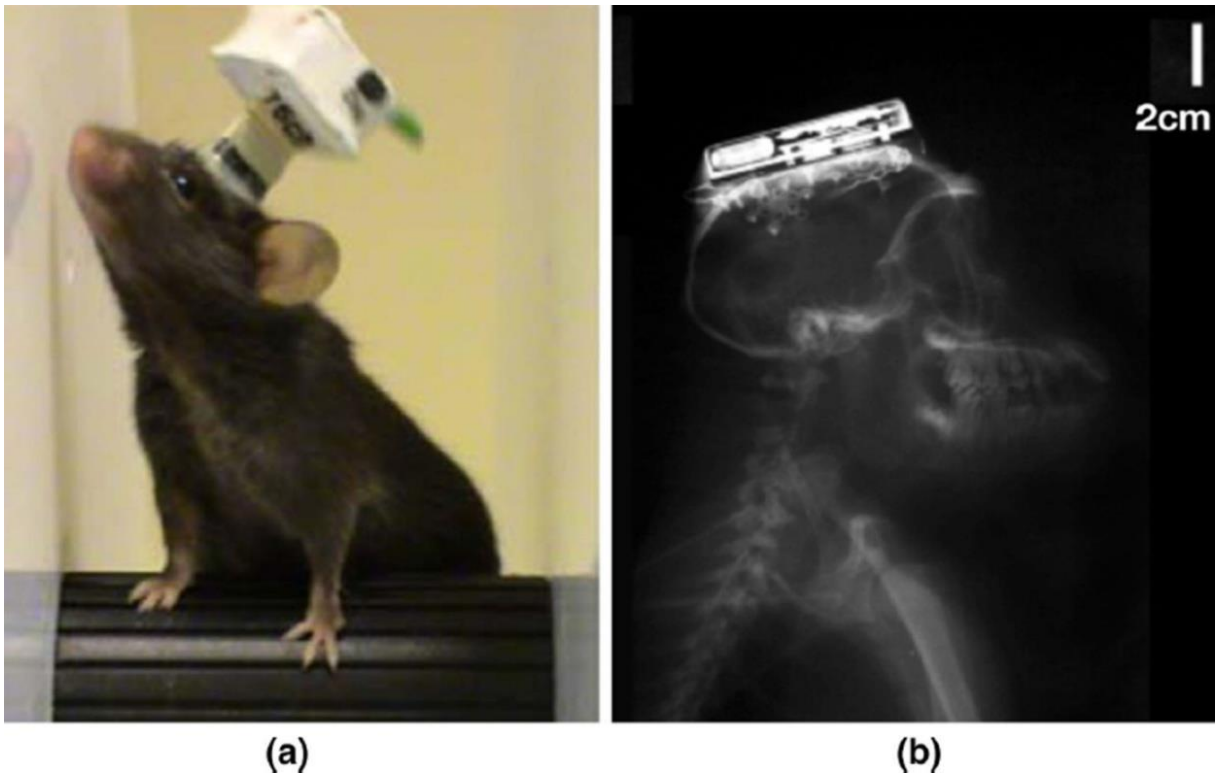


Fig.1.19: (a) *A neural recording system with an RF transceiver for brain studies in a rodent model, as reported by Fan et al. [64].* ***(b)*** *A similar system for performing CNS studies in a macaquemodel reported by Borton et al. [65]*

1.6.2 Applications in high energy physics experiments

The Front-End Electronics (FEE) for modern High Energy Physics Experiment (HEPE) is mixed-signal circuits, which perform precise measurement of particle trajectories (also arrival times and energy). Electrically pixel sensors that produce signals that are amplified in a sensitive element of the Front-End Electronic called charge sensitive amplifier (CSA) detect charged particles. Those pixel sensors are predominantly made of Silicon, a favourable material due to its relatively small band-gap of 1.12 eV with respect to the ionization energy of the older generation of gaseous detectors (typically more than 10 eV), and therefore, silicon sensors provide a relatively large signal. From the technology point of view, silicon is readily available and sensor fabrication process is compatible with the processes for fabrication of microelectronic circuits. When soft X-rays strike a semiconductor detector, free charges are generated [66, 67].

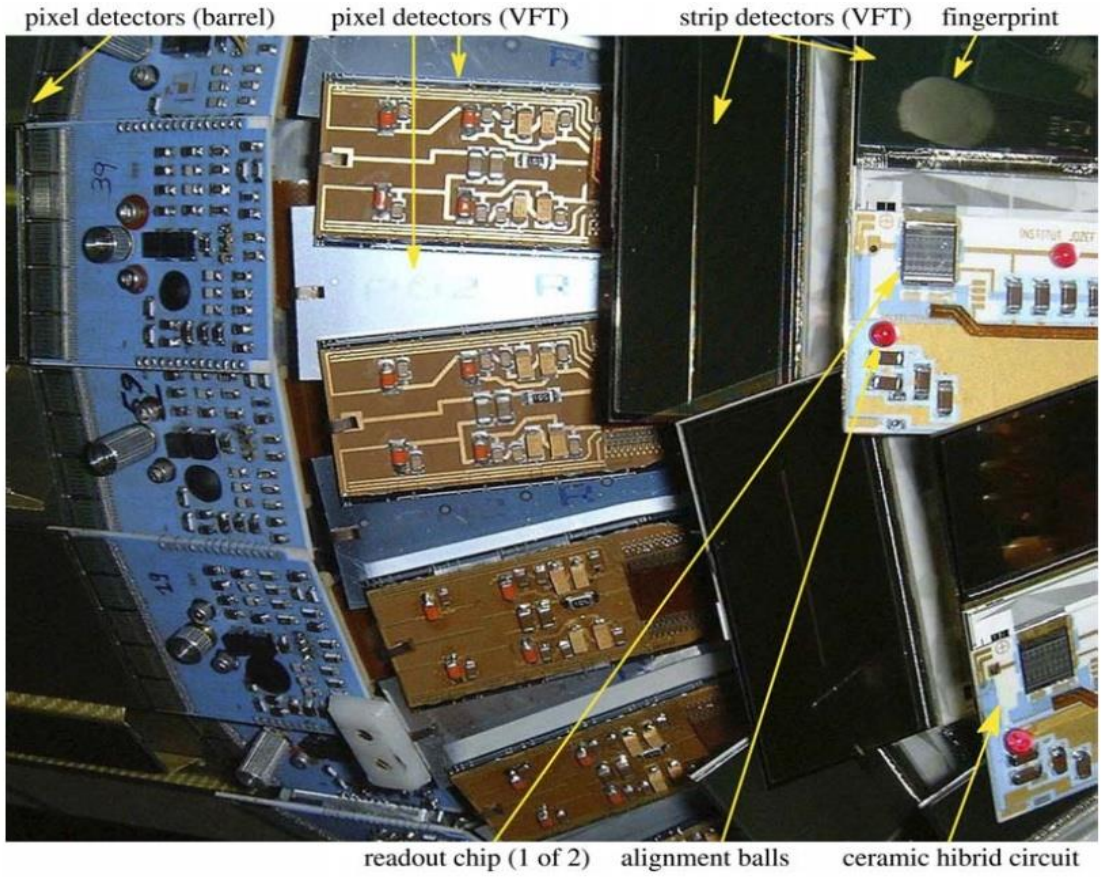


Figure.1.20. *Part of the Very Forward Tracker (VFT) mounted on both ends of the central Vertexdetector, as part of the upgrade of the DELPHI experiment of the old Large Electron–Positron (LEP) collider at CERN [68]*.

The strip detectors mounted in the Very Forward Tracker had a readout pitch of 200 µm and one interpolation strip between each readout pair. The detector area was 53×53 mm, thus allowing 256 readout channels per detector. Two MX6 chips, with 128 channels each performed the readout [69].

The Compact Muon Solenoid (CMS) illustrated in Fig.1.21[5], is predicted to receive a substantial upgrade of the outer tracker sensor and its front-end readout electronics, needing higher granularity and readout bandwidth to absorb a big amount of pileup events in the High-Luminosity Large Hadron Collider (LHC) [2, 5]. Therefore, the whole tracking system will be substituted with new sensors introducing higher radiation tolerance having capability of handling higher readout bandwidths and data rates [2, 5].

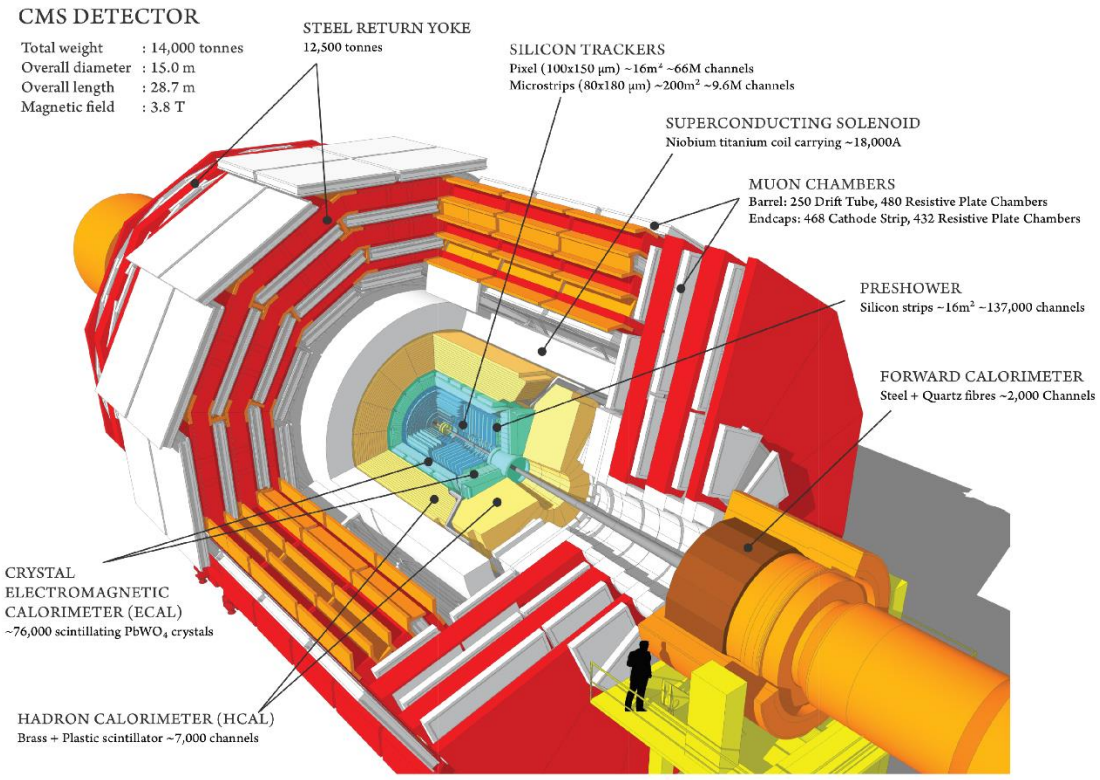


Figure.1.21. The building blocks of the Compact Muon Solenoid (CMS) [5].

To recognize particles having higher transverse momentum (> 2 GeV/c) and to distinguish the front-end output with a given L1 trigger level, a double layer sensor module, which combines a pixel sensor with a strip one, was adopted. Consequently, two different readout ASICs were developed, namely the Short Strip ASIC (SSA) for the strip sensor and the Macro Pixel ASIC (MPA) for the pixelated sensor [2, 5 and 6].

1.7 Conclusion

We reported in this chapter a review of literature on ASICs chip in readout systems based radiation detectors. Starting by some generalities on ASICs chip in radiation detection readout electronics, we have presented different architectures of ASICs that can be used in analog and digital systems. Some applications of ASICs have been discussed. Depending upon the type of detector and the particular application, the detected radiation can be read out event by event (e.g., in energy-resolving imagers and spectroscopic systems for research, security, safety, and medical applications) or it can be integrated from several events in the capacitance of the electrode and read out at a later time (e.g, in CCD or CMOS sensors for imaging and particle tracking) by a custom ASIC chip. The ionizing events, or photons, occur in most cases

randomly in time or, more rarely, during specific intervals, as in some high-energy physics experiments. Invariably, reading out the signals from radiation sensors requires highly specialized electronics, usually referred to as “front-end electronics (FEE)”. This electronics usually entails stringent requirements interms of the signal-to-noise ratio, dynamic range, linearity, stability, and resolution. In the next chapter, the design methodology and materials used in designing state-of-the-art front-end electronics for capacitive Silicon detectors is discussed and presented. The proposed FEE is then customized within a low-noise and low power ASIC for time and energy measurement of single photon silicon based detectors.

Chapter 2

MODELLING, NUMERICAL AND DESIGN METHODOLOGY

2.1 Introduction

Single photon detection readout ASICs are mostly used in many High Energy Physics Experiments (HEPE) for energy measurement and particle tracking. Detection of photons that has energy range of visible is relatively easy compared to detection of low and high energy photons outside of the visible range. In this chapter a complete ASIC chip for single photon detection systems and photon energy measurement, has been analyzed and designed. The circuit is dedicated to Silicon based detectors where the system guarantees high energy resolution and high counting rate (particle flux). The ASIC integrates a charge sensitive amplifier (CSA) with an adjustable gain stage for bandwidth compensation purpose, a fast pulse shaper (PS) which provides the energy deposited in the detector for every detected photon. The PS is followed by a discriminator which generates the trigger signal when the shaped pulse crosses a tunable threshold voltage reference. A fast trigger signal for time stamp is therefore customized. The completely ASIC is highlighted in Figure.2.1 bellow. Matlab base toolkit has been used for modelling and numerical simulations, furthermore spice simulations have been performed using LTspice and the silicon implementation of the chip was carried on using Electric VLSI which is an open source tools for integrated circuit design. This chapter is organized as follows: section 2.2 is dedicated to the analysis and design of the CSA. In section 2.3, the customized PS circuit is well described and designed for high counting rate purpose. Obviously, a trigger signal must be generated to identify the events. A discriminator based latch type comparator is used for generating a trigger signal, whenever the signal level at the output of the shaper is higher than a threshold level. In the following sections, we describe the operation and design of each block in detail. In section 2.4, a

detailed analysis of the discriminator based dynamic latch type comparator is performed. The chapter has been concluded in section 2.5.

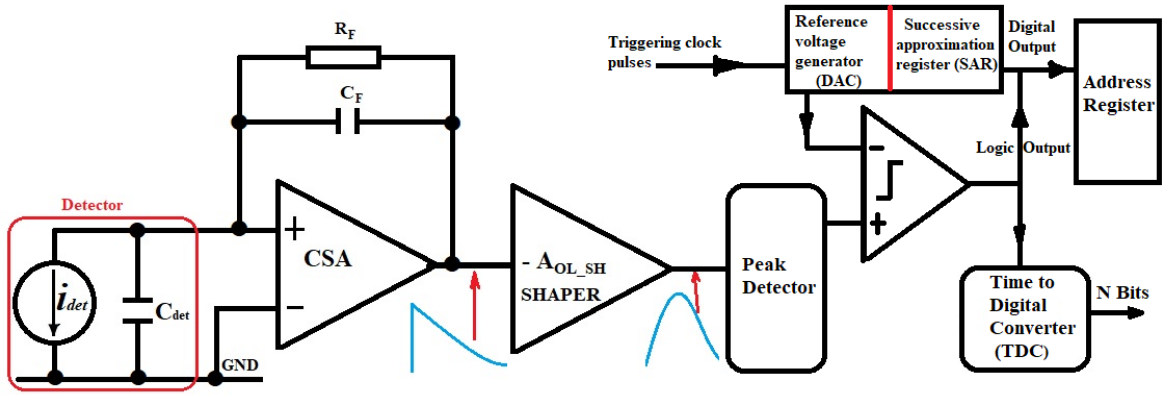


Figure.2.1: Global overview of a silicon based detector readout ASIC.

2.2. Design of the CSA amplifier circuit

2.2.1 Biasing point behavior and mismatch effects

For high-speed applications where a high counting rate is required, the *Gain BandWidth (GBW)* of the CSA must be made as large as possible [70, 71]. To overcome the bandwidth limitation and improve the amplitude resolution for excellent particles identification ability, the Gain BandWidth of our preamplifier is extended to achieve an output rise time about few ns as response to impulsive charge [70]. This requires therefore high input transistor transconductance (gm) [67], [73], and [74]. Most of the shortcomings of the previous section can be eliminated by custom transistor sizing during the design process [73], [75], [76], and [77] along with implementing an internal compensation. In the former case, the compensation network is fabricated on the chip, and usually, no external access to the compensation network is provided [78]. A custom compensation technique in which the CSA GBW is adjusted by an external device is proposed. The proposed CSA has been designed in 0.35 µm technology from Taiwan Semiconductor Manufacturing Company (TSMC) process. The input transistor aspect ratio *W/L* was suitable designed for low-noise and high gain purpose. Moreover an on-chip gain adjustable stage was implemented to extend the bandwidth of the core amplifier. This adjustable gain stage is controlled by an external resistor through a bias current. A custom feedback network was adapted to perform the initial conversion of small current pulses into voltage step pulses. Table.1. presents the design specifications of a CSA circuit for typical Silicon-PIN detector applications. In order to increase the gain of the CSA,

we studied a three-stage configuration for the design. The single-ended configuration of the circuit exhibited in Fig.2.3, is more appropriate than the differential one for the reduction of power consumption. The choice of the N-channel input transistor relies on the lower thermal noise compared to the P-type at high frequency, since the 1/f noise is negligible in the frequency region above 10 kHz [67], [79], [80]. In addition, N-channel MOS, gives a lower series white noise with respect to the P-channel counterpart, because of its higher transconductance [67], [79] at the same drain current compared to PMOS device. The current source at M_1's drain is provided by M_2, which is a P-channel MOSFET with smaller transconductance.

Table.1. CSA specifications required for silicon detector for two vendors [67]

VendorParameters	**Hamamatsu (H4083)**	**AMPTEK(A250)**
Power consumption	150 mW@12V	4 mW@6 V
Count rate	2.6 MHz	2.5 MHz
Detector capacitance	0 – 25 pF	0 – 250 pF
ENC (Cin = 5 pF)	240 e^-	6 e^-
Noise slope	4 e^-/pF	1.5 e^-/pF
Sensitivity	2 mV/MeV (Si)	176 mV/MeV (Si)
DC gain	94 dB	76 dB

The second stage is a common-source based current load, so that the drain current of M_8 (I_{bias}), is used to adjust the dc-gain of the amplifier. It utilizes a Miller Compensation combined with a custom feedback module for achieving good stability of the design. The stability of the preamplifier sensitivity is dependent on the stability of the feedback capacitor

(C_F is selected for good temperature stability) and the preamplifier open loop gain. The open loop gain will be very large so that small changes in the C_F can be neglected [81], [80].

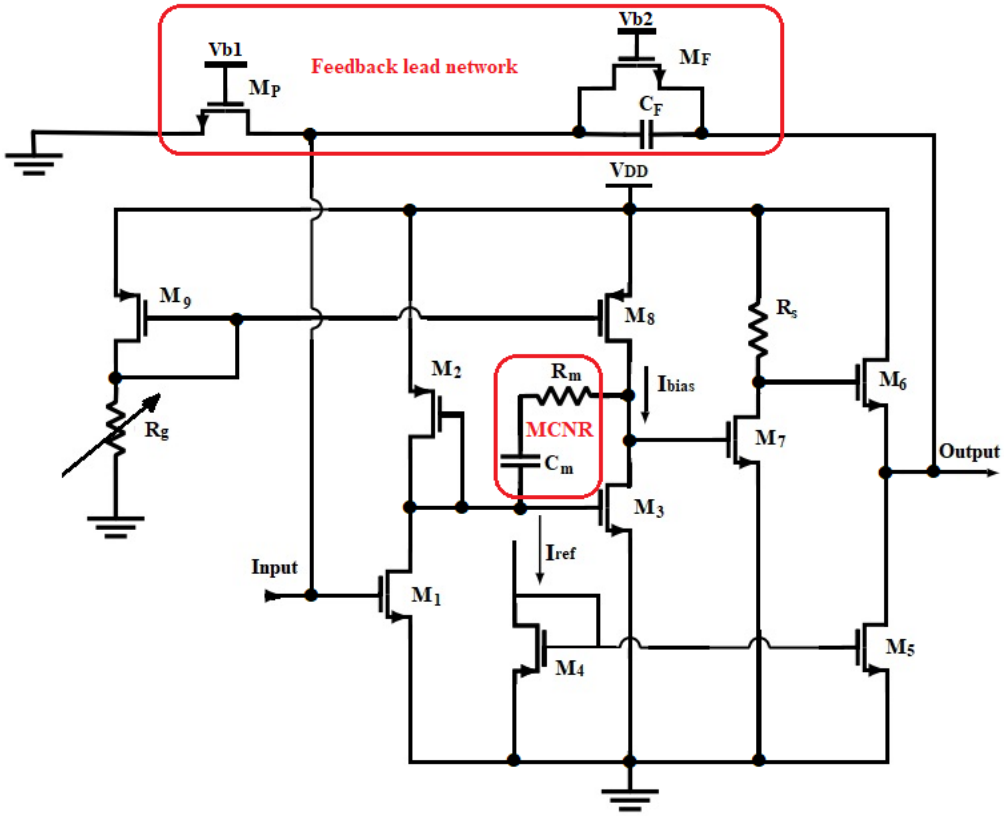


Figure.2.2 *Schematic structure of the proposed CSA.*

Therefore, the bias current is kept at a specific low value (2.5 µA) in order to keep very low transconductance of M_3 thus, exhibiting very high loop gain. Capacitor C_m provides a gain and the dominant pole in that stage; so, a resistance R_m is used to suppress direct transmission through C_m at high frequencies. Such a stage in the CSA incorporates a higher output resistance. The maximum signal swing must be kept limited so that all the transistors remain in their saturation state, i.e., $V_{GS} > V_T$ and $V_{DS} > V_{GS}-V_T$ [67], [81].

The third stage consists of an N-channel MOSFET M_7 which aims to give a negative gain of the entire circuit so that one can apply the negative feedback. It is biased by a low current through R_S. The value of Rs is set to 3 kΩ so that M_7 should operate in the saturation region. The output stage is a source follower based, designed to exhibit unity voltage gain. Current flow from M_4's drain kept M_5 biased in saturation. One of two inputs, feedback is connected to Vout through an on-chip feedback capacitor of 0.1 pF and a resistor of 3.54 MΩ at the top-

level design. The circuit was designed with thick oxide transistors that allow a relatively high supply voltage of 3.3 V in a standard 0.35 µm CMOS technology process. The achievable output rise time of the CSA circuit is given by $t_r = \frac{2.2}{2\pi GBW}$, where GBW is the gain bandwidth of the CSA core amplifier. From this formula, a fast pulse response of 7.36 ns was guaranteed for reaching 1 GHz gain bandwidth.

a- Analysis of the CSA core amplifier circuit

The first stage is a cascade topology developed based on a common source with diode-connected PMOS (M_2) so that the input is free from parasitic capacitance and the feedback amplifier controls the gate voltage.

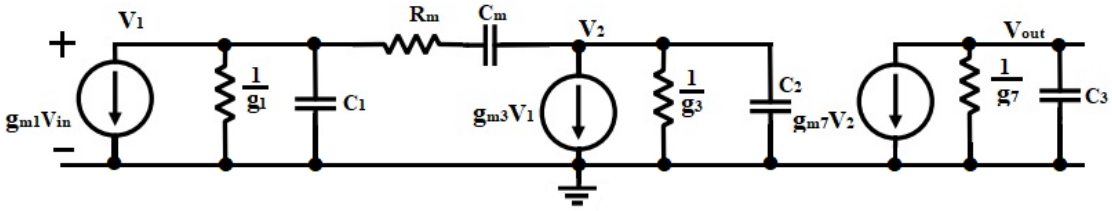


Figure.2.3: *Small-signal model of the core MCNR amplifier*

Therefore, the CSA input becomes a virtual ground and the detector capacitance is less significant to the CSA bandwidth. The specifications of the design impose to guaranty a high dc-gain and high stability. The small-signal analysis of the proposed circuit (Fig.2.3) results in the overall transfer function is presented as follows:

$$A(s) = \frac{A_{OLDC}\left(1 + C_m\left(R_m + 1/g_{m3}\right)s\right)}{\left(1 + \frac{g_{m3}g_{m7}r_{03}r_{o8}R_sC_m}{r_{03}+r_{o8}}s\right)\left(1 + C_m\frac{g_{m3}+g_{m7}}{g_{m3}g_{m7}}s + \frac{C_mC_L}{g_{m3}g_{m7}}s^2\right)} \quad (2.1)$$

where,g_{mi}, $r_{0i}$and C_i are denoted as the equivalent transconductance, output resistance and the lumped capacitance at the i[th] gain stage. The output parasitic capacitance being lumped in the load capacitance C_L.

$$\begin{cases} C_1 = C_{gd1} + C_{gd2} \\ C_2 = C_{gd3} + C_{gd8} + C_{gs7} \\ C_3 = C_{gd7} + C_{gd6} + C_L \end{cases} \quad (2.2)$$

To study the stability of the proposed design, the following assumptions are made to simplify the transfer function of the core amplifier. C_m and R_m being the Miller capacitor and the zero-nulling resistor respectively $C_3 \cong C_L and C_m$, $C_L >> C_1, C_2$ thus, (2.1) can be written as

$$A(s) = \frac{A_{OLDC}\left(1+\frac{s}{\omega_{z1}}\right)}{\left(1+\frac{s}{\omega_{po}}\right)\left(1+\frac{1}{Q}\frac{s}{\omega_{p1}}+\frac{s^2}{\omega^2_{p1}}\right)} \tag{2.3}$$

where the associated parameters are given by (2.4)

$$\begin{cases} \omega_{z1} = \dfrac{g_{m3}}{C_m\left(1+R_m g_{m3}\right)} \\ \omega_{po} = \dfrac{r_{03}+r_{o8}}{g_{m3}g_{m7}r_{03}r_{o8}R_s C_m} \\ \omega_{p1} = \sqrt{\dfrac{g_{m3}g_{m7}}{C_m C_L}} \\ A_{OLDC} = -\dfrac{g_{m1}g_{m3}g_{m7}r_{03}R_s}{g_{m2}\left(1+\lambda r_{03} I_{bias}\right)} \\ Q = \dfrac{\sqrt{g_{m3}g_{m7}}}{\left(g_{m3}+g_{m7}\right)}\sqrt{\dfrac{C_L}{C_m}} \end{cases} \tag{2.4}$$

However, the dc-gain (A_{OLDC}) of the circuit as depicted in (4) depends on I_{bias} and can be adjusted by an external resistor Rg; λ being the channel modulation parameter. The system's phase margin (PM) with pole zero cancellation is given by (2.5)

$$PM = \tan^{-1}\left(\frac{GBW}{\omega_{z1}}\right) - \tan^{-1}\left(\frac{GBW/\omega_{po}}{Q\left(1-\left(GBW/\omega_{po}\right)^2\right)}\right) \tag{2.5}$$

A MATLAB based toolkit has been developed in order to simplifiy the design [10]. The scripts in the toolkit use small-signal parameters of the transistors and the parasitic capacitances as input data to assist in designing the three-stage opamps. Fig.2.3 illustrates the frequency response of a Miller compensation nulling resistor (MCNR) three-stage Opamp designed for 42° phase-margin (black line). It is evident that the amplifier exibited two poles;

the dominant pole ω_{po}, the large pole ω_{p1} and one zero, all associated to equation (2.3). The poles are located at 74.6 kHz and 141.42 MHz respectively; and the zero is situated at the frequency of 998 MHz. The feedback network is designed to introduce a phase lead near the crossover frequency, thus cancelling the second pole of the Open-loop gain (OLG) which is located at the frequency of 141.42 MHz; then, increases the amplifier's phase margin. The transfer function associated to the feedback network is written as:

$$\begin{cases} K(s) = \dfrac{K\left(1+\tau_F s\right)}{\left(1+\tau_p s\right)} \\ \tau_F = R_F C_F \\ \tau_p = K\tau_F \\ K = \dfrac{R_P}{R_P + R_F} \end{cases} \tag{2.6}$$

b- Feedback leads network (FLN) implementation

This module consists of a charge collecting capacitor C_F and active network resistors (M_P and M_F) based voltage controlled NMOS resistor. The value of C_F was chosen to ensure sufficient high charge-gain conversion that will prevent the design against saturation. In fact, in most conventional CSA design, the charge gain needs to be low enough to keep the preamplifier output from saturation. Since, saturating the output would cause ballistic deficit, which is a reduction in amplitude because the bandwidth has been degraded by the gain [75]. In this design, the bandwidth compensation is achieved thanks to the adjusted gain stage. Therefore, a feedback capacitor of 0.1 pF was set to handle a maximum input charge of 280 fC, without compromising the bandwidth. To minimize the feedback area, M_P and M_F are based on a NMOS transistor working in linear region; their channel dimensions ratios are sized to exhibit no parallel noise. However, biasing the feedback network is a challenge because in order to achieve a large effective resistance the operating region of the MOSFETs is of interest. Considering a MOS device biased in strong inversion and working in the linear region, the drain-source current characteristics can be written as:

$$I_{DS} = \mu_n C_{ox} R_d \left[(V_{GS} - V_{THN})V_{DS} - \frac{{V_{DS}}^2}{2}\right] \tag{2.7}$$

Hence, M_P being biased to operate in triode region, and neglecting the channel length modulation and the quadratic effect of the drain-source voltage, the equivalent resistor of the NMOS device is given as:

$$R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{THN})} \quad (2.8)$$

M_P being designed to handle 1.42 kΩ equivalant resistor with $\left(\frac{W}{L}\right)_P = \frac{2.772\,\mu}{0.7\,\mu}$. However based on equation (2.8), M_F was biased to operate in weak inversion moderate with $\left(\frac{W}{L}\right)_F = \frac{3\,\mu}{36\,\mu}$. This allows achieving very large equivalent resistance of 3.542 MΩ.

2.2. Design of the CR-RC[1] pulse shaper circuit

In order to optimize the signal-to-noise ratio (SNR) of the detector readout electronics and reduce the signal interference between signals from different time, the output signal of the CSA is needed to be shaped using a first order active CR-RC pulse shaper (PS) circuit as illustrated in **Fig.2.4**. Low-frequency noise (1/f) and thermal (high-frequency) noise was suppressed using custom shaper circuit consisting of a differentiator and an integrator with constant time both equal to the optimal shaping time ($\tau_d = \tau_i = \tau_{s,opt}$). The pulse shaper circuit provides an output voltage proportional to the energy of the detected particles. The topology of the core amplifier used in the CSA is used for the purpose. Therefore, loop gain $A_{\mathrm{OL\_SH}}$ of the PS is given by (2.16) as follows:

$$A_{OL\_SH} = \frac{\Delta V_{CSA,max}}{\Delta Q_{max}} C_F \left(\frac{e}{n}\right)^n n! \quad (2.9)$$

where n is the order of the shaper. Using the design parameters, allows achieving 2.67 loop gain. It is easy to derive the shaping design parameters as follows: $C_d R_d = C_i R_i$ and $\frac{R_d}{R_i} = \frac{C_d}{C_i} = \frac{1}{A_{OL\_SH}}$. For 200 fF integrating capacitor, $C_d = 534\,fF, R_d$ =400.75 kΩ and R_i =1.07 MΩ respectively.

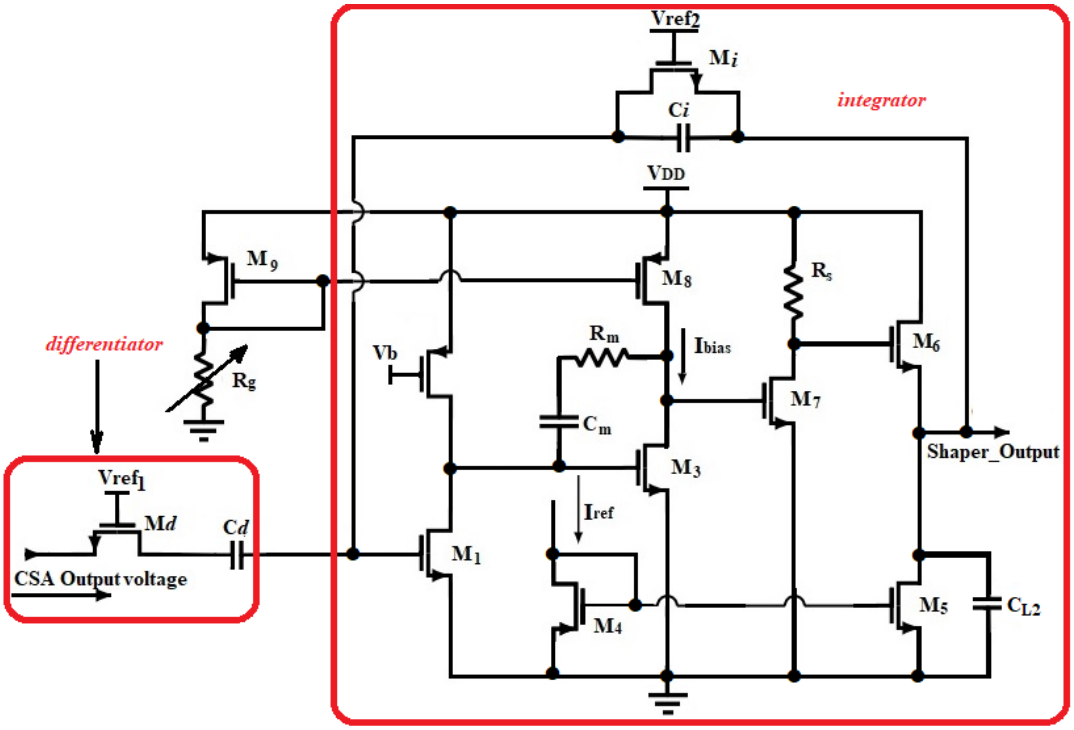


Figure.2.4: *Schematic of the proposed structure of the Shaper.*

Henceforth, R_d and R_i are very large, thus should occupy more space. Using (8) with suitable transistor biasing within the design process, the equivalent resistance can be derived from NMOS device operating in weak inversion moderate so that $\frac{W_i}{L_i} = \frac{10\,\mu}{41\,\mu}$, $V_{GSi} = 0.7\,V$ and $\frac{W_d}{L_d} = \frac{2\,\mu}{23.6\,\mu}$, V_{GSd} =0.9 V. However, the PS core amplifier would exhibit a gain-bandwidth given by $GBW_{SH} = \frac{1}{2\pi\tau_{s,opt}} = 744.1\,kHz.$ Hence, $GBW_{SH} = \frac{g_{m1sh}}{2\pi C_{L2}}$, g_{m1sh} being the transconductance of the input transistor and C_{L2} the total load capacitance of the shaper. For 1pF, load capacitance, the small-signal transconductance is calculated from the previous expressions and controlled to be 4.67 μS, which allow simulating 91.2 nA drain-source current, exhibiting therefore an ultra-low power dissipation of only 0.301 µW, while the geometric aspect ratio of the device was controlled at $\frac{W_{sh1}}{L_{sh1}} = \frac{3\,\mu}{20\,\mu}$. Moreover, the shaper input stage was chosen to be a common source with P-channel MOSFET active load. The former device was biased to work in strong inversion saturation regime by $V_b = 1.2\,V$, and adjusted to handle $A_{OL\_SH} = -10$ input gain stage, so $g_{m2sh} = \frac{g_{m1sh}}{10}$.

2.4. Noise analysis of the analog front-end

The noise sources are mainly from detectors, preamplifiers and shapers. The CSA, along with providing low-noise amplification, offer low input impedance (virtual ground) which stabilizes the potential of the sensor electrode and reduces the inter-electrode cross talk [82]. The input transistor of the CSA being designed to operate in strong inversion saturation and optimized to handle the lowest possible equivalent noise charge (ENC). The total ENC_{CSA} for a given feedback and detector capacitor, according to the adopted CMOS process consist of three different components [67] and given as follows:

- The most prominent thermal noise contribution can be calculated as:

$$ENC_{th}{}^2 = \frac{4K_BTn\gamma\alpha_n}{q^2}\frac{(C_{det}+C_f+C_g)^2}{g_mC_g}\frac{N_{th}}{\tau_s} \quad (2.10)$$

where K_B is the Boltzmann constant, T is the room temperature, η is the body factor, γ is the inversion factor, α_n the excess noise factor, N_{th} is the shaper noise index for the thermal noise, $\tau_s$is the peaking time, C_{det} the detector capacitance, C_f the feedback capacitor, C_g the gate capacitance and g_m is the input MOSFET transconductance.

- The flicker noise or the noise due to 1/f is expressed as:

$$ENC_{1/f}{}^2 = \frac{K_f}{q^2}\frac{(C_{det}+C_f+C_g)^2}{C_g}N_f \quad (2.11)$$

Where K_f *is* the flicker noise coefficient N_f and the shaper noise index for flicker noise

- The white parallel noise contribution due to the detector leakage current (I_{leak}), the MOSFET gate current and feedback resistor R_f, is defined as follows:

$$ENC_i{}^2 = 2q(I_{leak} + I_G)N_i\tau_s + \frac{4K_BTN_i}{q^2R_f} \quad (2.12)$$

where q is the elementary charge, I_G the gate current of the input transistor, R_f the feedback resistance and N_i and the shaper noise index for the white noise. Different components of the ENC were first optimized with respect to W and I_D, and then respect to C_g [67] using a first order shaper. The optimization technique well explained in ref [67 and83] is therefore adopted and the optimized parameters are derived as follows $W_{opt} = \frac{3(C_{det}+C_f)}{2C_{ox}L_{min}}$ and $I_{D,opt} = \frac{g_m{}^2L_{min}}{2\mu_nC_{ox}W_{opt}}$. The instability of the drain current (I_D) is established by the variation of charge in the depletion region, which constitutes the channel width. L_{min} and W_{opt} are the minimal length and the optimal width of the input device. W_{opt}, being calculated at 62.5 μm and $L_{min} = 10.5\,\mu m$ the design requirements allow achieving very much less drain

currentof$I_{D,opt} = 2.5\ \mu A$, for the CSA input transistor. Since the bias current of M1 is fixed to its optimal value, increasing *W/L* reduces the overdrive voltage V_{GS}-V_{TH}, eventually driving the transistor in moderate or weak inversion. Therefore, if the transistor works in this region, increasing its gate width too much worsens the noise, because it leads to more gate capacitance without improving the transconductance [67 and 84]. The total gate capacitance, which optimizes the different components of ENC, is obtained by solving the equations $\frac{\partial ENC_{th}{}^2}{\partial C_g} = 0$ and $\frac{\partial ENC_{1/f}{}^2}{\partial C_g} = 0$ respectively [67].The solutions of those equations are found to be:

$$C_{g,th} = \frac{3}{2}\left(C_{det} + C_f\right) \text{ and } C_{g,1/f} = \left(C_{det} + C_f\right) \qquad (2.13)$$

The values of the gate capacitances given by (16), limit the operating regime of the input device. The gate width is finally adjusted to achieve the matching condition defined in (16). At this point, if the contribution of the ENC due to flicker noise is greater than the one given by thermal noise, *Cg* can be further increased. Depending on the value of K_f and the peaking time, the optimization will result in a *W* yielding a gate capacitance between $\frac{3}{2}\left(C_{det} + C_f\right)$ and $\left(C_{det} + C_f\right)$. Hence, the input capacitance must be much greater than the other sources of capacitance connected to the preamplifier input in order for the preamplifier sensitivity to be unaffected by external capacitance changes [73]. Considering the input transistor in the strong inversion saturation mode, W_{opt} leads to $C_{g,opt} = \left(C_{det} + C_f\right)$. Thus, in this regime, the same value of gate capacitance minimizes both flicker and thermal noise. Therefore, from equations (12), (13) and (14) the total ENC of the CSA can be expressed as:

$$ENC_{CSA} = \frac{1}{q}\left(\left(\sqrt{\frac{A_1}{g_{m1}\tau_p}} + \sqrt{A_2}\right)\left(C_{det} + C_f\right) + \left(q(I_{leak} + I_G)\tau_s + \frac{4K_BT}{R_F}\right)N_i\right) \qquad (2.14)$$

where, $A_1 = \frac{K_B T n \gamma \alpha_n}{3} N_{th}$ and $A_2 = \frac{16 K_f N_f}{3}$.

However, the passive feedback resistance (R_f) is replaced by the voltage controlled NMOS resistor network, which exhibited no parallel resistive noise. Moreover, the optimal shaping time is obtained solving equation $\frac{\partial ENC_{total}{}^2}{\partial \tau_p} = 0$. Thus (2.16) gives optimal shaping time and the optimized ENC is given by (2.17).

$$\tau_{s,opt} = \sqrt{\frac{A_1}{q I_{leak} g_{m1} N_i}}\left(C_{det} + C_f\right) \qquad (2.16)$$

$$ENC_{CSA} = \frac{1}{q}\left(\left(\sqrt{\frac{A_1}{g_{m1}\tau_{s,opt}}} + \sqrt{A_2}\right)\left(C_{det} + C_f\right) + \left(q(I_{leak} + I_G)\tau_{s,opt} + \frac{4K_BT}{R_F}\right)N_i\right) \quad (2.17)$$

Assuming that the shaper amplifiers are characterized by infinite gain and are noiseless, the noise contribution from the amplifiers can be made negligible by increasing the size and power of the active devices [67], [85]. The ENC contribution of the shaper comes from the dissipative feedback component [86]. The parallel noise spectral can be reported as an equivalent parallel noise generator at the input of the charge amplifier by scaling it with the square of the charge gain of the shaper A_{OL_SH} [67], [85], and [87]. Thus, the shaper ENC component is given as:

$$ENC_{SH}{}^2 = \frac{4K_BT}{A_{OL\_SH}{}^2 R_i} N_p \tau_s \quad (2.18)$$

where, N_p is the ENC coefficient for white parallel noise [84].

The total equivalent noise charge of the front-end electronic, defined as the quadratic sum of the CSA and the shaper components can be expressed as follows:

$$ENC_{total} = \sqrt{\frac{1}{q^2}\left(\left(\sqrt{\frac{A_1}{g_{m1}\tau_{s,opt}}} + \sqrt{A_2}\right)\left(C_{det} + C_f\right) + \left(q(I_{leak} + I_G)\tau_{s,opt} + \frac{4K_BT}{R_F}\right)N_i\right)^2 + \frac{4K_BT}{A_{OL\_SH}{}^2 R_i} N_p \tau_{s,opt}} \quad (2.19)$$

A pole zero canceller (PZC), which allows canceling out the pole created at the output of the CSA circuit connects the analog module (CSA + PS) circuits. The output of the PS is connected to a fast discriminator based latch type comparator to generate a trigger, which allows building the gate logic of the circuit.

2.5 Discriminator system

Pulse height discriminators are used to generate trigger signals for the channels with incidents. Ideally, a discriminator must deliver a logic signal that distinguishes if the front-end output is below or above a given threshold. This information is then passed to a digital control machine that takes the appropriate decisions on the following signal processing and/or data transmission steps. The discriminator output has therefore two possible states, one corresponding to the logic level “zero” (0 V in a single supply system) and the other to the logic level “one” (in general equal to V_{DD}), and switches instantaneously between the two

states when the threshold is crossed. The discrimination principle used in this thesis for single photon detection is well described. The system consisted of a fast comparator, which aims to detect a pulse event (photon. A logic module is used to handle the photon arrival and the memorization process. The effects of gain and speed limitations in practical circuits must thus be considered.

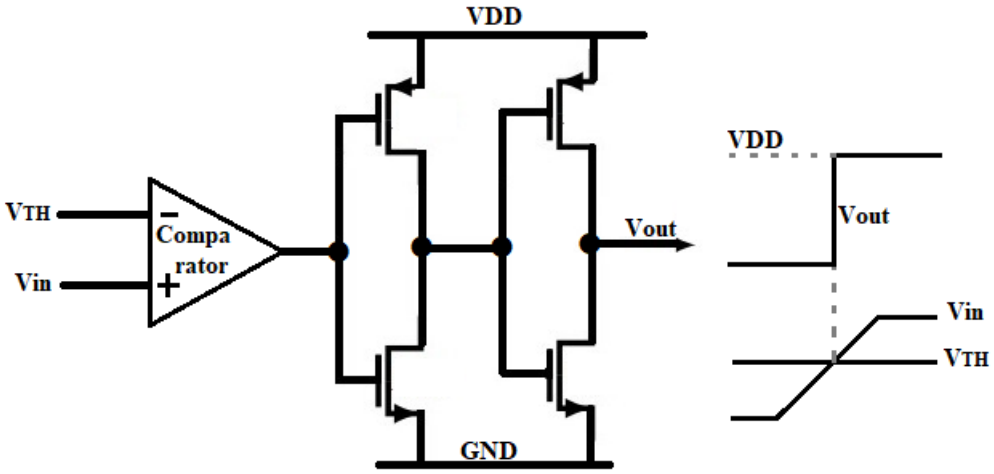


Fig.2.5. Conceptual scheme of a voltage discriminator with its idealized response.

As shown in Fig.2.5, a discriminator consists of a high gain differential voltage amplifier followed by a chain of CMOS digital inverters. The output gates serve two purposes: on the one hand, they ensure that the comparator delivers to the following digital stage a well-defined logic signal. On the other, they provide adequate buffering power to drive the output load. The number of inverters shown in the figure is only indicative and the output stage needs to be optimized according to the load the circuit is expected to drive. In case the comparator output needs to be fanned out to multiple destinations, a buffer with more stages than that shown in Fig.257can be required. If the output load is small, oversizing the buffer is unnecessary and leads to additional power consumption and to a higher risk of coupling digital noise into the front-end.

2.5.1 Proposed dynamic latch comparator

The proposed dynamic latch comparator utilizes a differential pair amplifier with enhancement NMOS load to achieve sufficient gain for low offset and high-speed solution as depicted in Fig.2.6. Therefore, the gain of this comparator will be high due to using the enhanced differential amplifier, which leads to improving the power consumption and the

comparison speed [95], [96]. In fact, NMOS load transistor's source swing from 0 to V_{DD} - V_{THN} when its gate and drain are clocked from 0 to V_{DD}; comparing to the PMOS counterpart which nodes swing from 0 to V_{DD}. So, the differential output nodes (F1 and F2) should be pre-charged from 0 to V_{DD} - V_{THN}. Furthermore, for NMOS, the V_{TH} is increased when its body-source voltage is biased to be negative. This is referred to as reverse body biasing (RBB) [96]. The variability of V_{THP} and V_{THN} (in PMOS and NMOS transistors) tends to be quite high in nano-meter CMOS technologies [97]. Thus, it must be kept as low as possible through proper transistor sizing in order to reduce the body effect which lowers the voltage swing at the preamplifier output nodes.

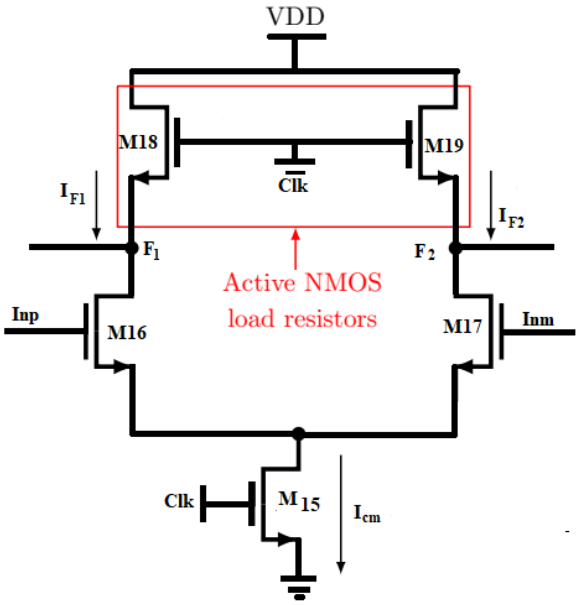


Figure.2.6: *Block diagram of proposed preamplifier with enhancement NMOS load*

The rest of the circuit consists of a decision circuit (latch) as depicted on Fig.2.7, and an output. The whole circuit works into two phases: reset or pre-charge phase and regeneration or Evaluation phase.

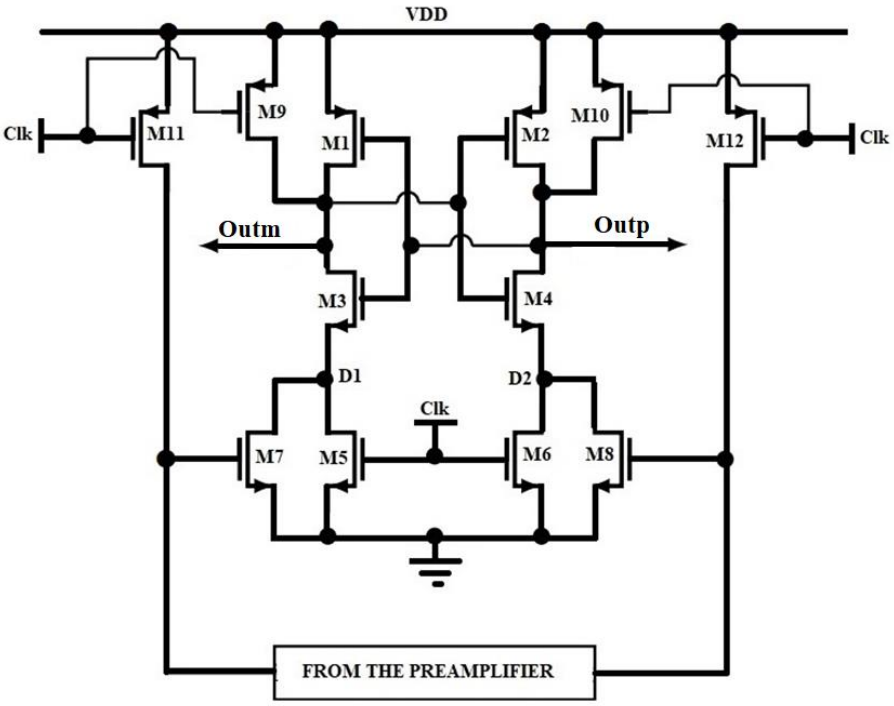


Figure.2.7: Block diagram of the proposed Dynamic Latch Comparator (Latch circuit)

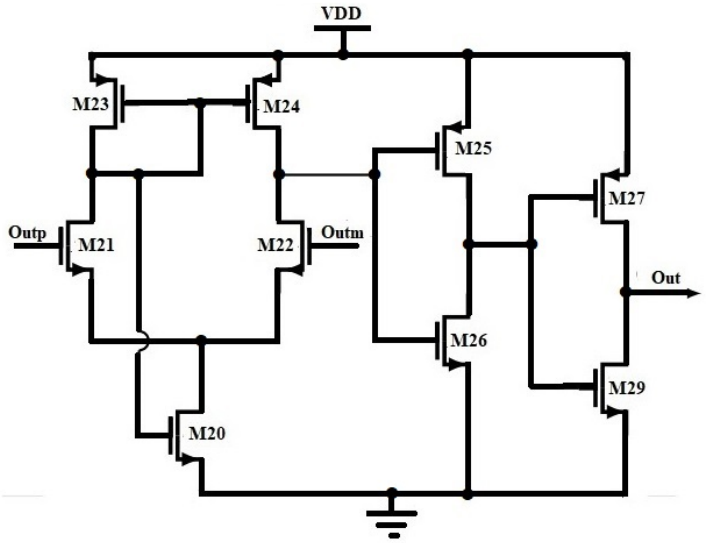


Figure.2.8: Block diagram of the output buffer of the proposed Dynamic Latch Comparator

a- The reset phase or pre-charge

In the reset phase, the clock is low; the tail transistor of the sense amplifier (M15) is off. Therefore, the current source of M15 is switched off; ensuring that there is no static power consumption in the first phase. Nevertheless, M19 and M18 are ON, pulling terminal F1 and F2 to V_{DD} -V_{THN} . As a result, M7 and M8 turn ON. Since M5 and M6 are off; M7 and M8

ON; nodes D1 and D2 are discharged to ground. The pull-up transistors (M9 and M10) of the latch are ON so, the output nodes Outp and Outm are pre-charged to V_{DD}.

b- The regeneration or evaluation phase

M19, M18, M9, M10, M11 and M12 are Off. Therefore, M4 and M3 begin to conduct. Since Vinp> V inm, the drain voltage of M16 started to fall at a faster rate than the drain of M17 due to the highest transconductance of M16 comparing to M17. The tail transistor of the sense amplifier is ON and begins to conduct. Therefore, the positive feedback from the cross-coupled M2, M3 kicks in; the node D1 drops faster and pulls Voutm to low logic; therefore M2 turns ON and pulls Voutp to high logic. Ones the decision made, comparator outputs control M4 and M3, which will be turn off to avoid static power dissipation. The opposite effect occurs when Vinm>Vinp; in that case Voutp is pulled to low logic and Voutm to high logic. To reduce the kickback noise due to the transient at the regeneration nodes D1 and D2, the drains of the transistors forming the input differential pair need to be isolated from the regeneration nodes during the regeneration phase. This is done using switching transistors M7 and M8 between the regeneration node and the drains of the input differential pair. These switches isolate the regeneration node and the drains of the input differential pair when regeneration starts. However, offset voltage is reduced using custom transistor sizing/matching during the design process, to avoid mismatch and process variation. Suitable transistor sizing was performed in order to obtain very small offset voltage at the input common mode voltage of 0.5 V. As depicted on that figure, the comparator will become very slow and its outputs may not settle to a valid level. In fact, the differential input voltage is set to 5 mV, that value is very small and closed to the offset voltage; this affects the time response of the circuit, which enters in a metastable state. Metastability is a problem that occurs in all latching comparators when the input is near the comparator decision point. That phenomenon is mostly due to parasitic; the inter connects between the transistors and the bulk silicon include many parasitic capacitances. Those capacitances, particularly at the nodes with the positive feedback of the latch (M2, M3), are seriously influencing metastability and the regeneration process. To avoid that, we used a symmetrical placement of all the transistors while laying-out the design [98], the enhancement NMOS load in the preamplifier stage, and all the other NMOS transistors of the circuit were designed to handle a zero potential between the source and substrate. This will reduce at a great extent the source-substrate parasitic capacitance and therefore lowering the probability of having meta-stabilities.

2.5.2 Analysis of the time delay of the proposed Dynamic Latch Comparator

The total delay time in this design is the sum of two components; the delay of the load capacitive discharge (t_{dis}) which is the period from the rising edge of the clock to the time when Outp and Outm are charged to V_{THN}; and the delay of the latch due to the regeneration (t_{latch}).

$$\boldsymbol{t_{delay} = t_{dis} + t_{latch}} \quad (2.20)$$

$$t_{dis} = \frac{V_{THN} C_{out}}{I_p} = \frac{2V_{THN} C_{out} \mu_p C_{ox} \frac{W_p}{L_p}}{g_{m,eff}^2} \quad (2.21)$$

$$g_{m,eff} = g_{mp} + g_{mn} = g_{mp}\left(1 + \frac{g_{mn}}{g_{mp}}\right) \quad (2.22)$$

$$g_{mp} = \mu_p C_{ox} \frac{W_p}{L_p} (|V_{GSP}| - V_{THP}) \quad (2.23)$$

$$g_{mp} = \mu_n C_{ox} \frac{W_n}{L_n} (V_{GSN} - V_{THN}) \quad (2.24)$$

therefore, t_{dis} can be calculated as;

$$t_{dis} = \frac{2V_{THN} C_{out} \mu_p C_{ox} \frac{W_p}{L_p}}{g_{mp}^2 \left(1+\frac{g_{mn}}{g_{mp}}\right)^2} = \frac{t_0}{\left(1+\frac{g_{mn}}{g_{mp}}\right)^2} \quad (2.25)$$

Wheret_0, is the period from the rising edge of the clock to the time when Outp and Outm are charged to V_{THN} considered in the conventional DLC [99]. However, the delay of the latch is given by equation (2.26) as

$$t_{latch} = \frac{C_{out}}{g_{m,eff} + g_{m11,12}} ln\left(\frac{\Delta V_{out}}{\Delta V_0}\right) \quad (2.26)$$

Where $\Delta V_{out} = \frac{V_{DD}}{2}$ and $g_{m,eff}$ is the effective transconductance of the back-to-back inverter, and ΔV_0 is the difference of the initial output voltage of the latch at the beginning of the regeneration.

$$\Delta V_0 = g_{m17,16}\left(g_{m5,6} + g_{m7,8}\right) \frac{\Delta V_{in}}{C_{out}} t_{dis} \quad (2.27)$$

Equations (2.26) and (2.27) lead to the following formula:

$$t_{delay} = \frac{t_0}{\left(1+\frac{g_{mn}}{g_{mp}}\right)^2} + \frac{C_{out}}{g_{m,eff} + g_{m11,12}} ln\left(\frac{\frac{V_{DD}}{2}\left(1+\frac{g_{mn}}{g_{mp}}\right)^2}{g_{m17,16}\left(g_{m5,6} + g_{m7,8}\right)\frac{\Delta V_{in}}{C_{out}} t_0}\right) \quad (2.28)$$

Further computations of (2.28) lead to the developed expression of the total time delay given as:

$$t_{delay} = \frac{t_0}{\left(1+\frac{g_{mn}}{g_{mp}}\right)^2} + \frac{t_{latch}}{1+\frac{g_{m11,12}}{g_{meff}}} + \frac{2C_{out}}{g_{m,eff}+g_{m11,12}} ln\left(\frac{1+\frac{g_{mn}}{g_{mp}}}{g_{m17,16}(g_{m5,6}+ g_{m7,8})}\right) \quad (2.29)$$

$t_0$and t_{latch} being the delay of the pre-charge and the evaluation phases respectively in the Conventional Double Tail Comparator (CDTC) and the comparator in ref [100]. In this equation, the third term has a negative contribution since, $M_{5\text{-}8}$, M_{16} and M_{17} are designed so that, $g_{m17,16}(g_{m5,6} + g_{m7,8}) > 1 + \frac{g_{mn}}{g_{mp}}$. Therefore, the total delay is reduced at a great extent.

Equation (2.29) represents the effect of various parameters on the total delay time. As depicted in that equation, the time delay of the preamplifier in the proposed structure is a fraction of the corresponding delay for the conventional structure. For a better optimization of time delay, furthers analysis should be carried on depending on the correlation between time delay and each of those parameters [100].

2.5.1 Noise analysis of the proposed latch comparator

2.5.3.1 Kickback noise analysis

When the regeneration phase starts, the switch opens and the two cross-coupled inverters implement a positive feedback; this makes the output voltages go towards 0 and V_{DD}, according to the small output voltage found at the end of the reset phase. Bessides, the effects of the internal capacitances of the MOS devices and local mismatch on transistors can exacerbate the situation [101]. The input voltage is disturbed, which may degrade the accuracy of the converter. This disturbance is usually called kickback noise. Generally, high-speed and high power-efficient comparators generate more kickback noise [102], [103]. The proposed comparator exhibited high speed and low kickback noise due to using the auxiliary transistors M5, M6, M7, and M8 to isolate the preamplifier output nodes first, and secondly reducing mismatch effect and parasitic capacitance of the transistors while designing the devices.

2.5.3.2 Thermal Noise

The proposed enhanced differential pair which devices operate in weak inversion mode exhibited high gain, provided by $g_{m16,17}$. There is a possible increase of input noise at the differential input therefore [103]. During the evaluation phase, M19, M18, M9, M10, M11 and M12 are Off; so do not contribute to the noise behaviour of the proposed circuit.

However, M1-M4 devices are cascaded, so their noise effect is negligible at low frequencies [104]. Thus, the total input referred noise voltage of the comparator consists of M5-M8, M16/M17 noise contribution. M16/M17 devices are sized identically to produce the same/similar input referred offset [105]. The input referred noise of those devices consisting the input differential amplifier for weak inversion operation is well analysed in ref [105] and given at a time t=*Tint* as:

$$v_{n,th,in}^2(T_{int}) = \frac{2nkT}{C_L \Delta V_{Fi,cm}(T_{int}) \left(\frac{g_{m17,16}}{I_{cm}}\right)_{T_{int}}} \quad (2.30)$$

where, n, is a process constant, $I_{cm}(t)$ is the tail current, T_{int} the integration time, k the Boltzmann constant and T is Kelvin's temperature.

Moreover, M7-M8 can be seen as complementary input which thermal noise can be modelled as a voltage source in series with the input. Thus, exploiting the analysis given in ref [103, 104], the thermal noise contribution of M5-M8 at the output of the comparator is given as:

$$\begin{aligned} V_{n,th,out}^2(T_{int}) &= \left(I_{n,th,5}^2 + I_{n,th,6}^2 + I_{n,th,7}^2 + I_{n,th,8}^2\right) R_{out}^2 \\ &= 8kT\gamma(g_{m5,6} + g_{m7,8})R_{out}^2 \end{aligned} \quad (2.31)$$

where, γ is the channel thermal coefficient and R_{out} the output impedance of the latch system. The input referred noise for M5-M8 can be derived as,

$$V_{n,th,in}^2(T_{int}) = \frac{V_{n,th,out}^2(T_{int})}{A_{latch}^2} \quad (2.32)$$

where A_{latch} is the voltage gain of the latch. Hence, considering the operating state of each transistor in the evaluation phase, the latch gain can be given as,

$$A_{latch} = (g_{m5,6} + g_{m7,8})\, R_{out} \quad (2.33)$$

Substituting A_{latch} from (2.33), equation (2.32) leads to

$$V_{n,th,in}^2(T_{int}) = \frac{8kT\gamma}{(g_{m5,6} + g_{m7,8})} \quad (2.34)$$

By adding those two (from 2.30 and 2.34) components, the total input referred noise of the designed comparator is given as:

$$E_{n,th,in}^2(T_{int}) = \frac{2nkT}{C_L \Delta V_{Fi,cm}(T_{int}) \left(\frac{g_{m17,16}}{I_{cm}}\right)_{T_{int}}} + \frac{8kT\gamma}{(g_{m5,6} + g_{m7,8})} \quad (2.35)$$

As highlighted in equation (2.41), it is evident that a large $\left(\frac{g_{m17,16}}{I_{cm}}\right)$ combined with a large $g_{m5,6}$ & $g_{m7,8}$, is needed for improving the noise performance of our proposed design. To get the lowest possible noise at a given current, it is desirable to maximize $\left(\frac{g_m}{I_{cm}}\right)$ for the

differential input, which means that it is desirable to let M16 and M17 operate in weak inversion until the latch stage makes decision [104, 105]. It can be concluded that by using the auxiliary devices sized to keep their transconductance sufficiently high and increasing $\left(\frac{g_{m17,16}}{I_{cm}}\right)$ for the differential input amplifier, the thermal noise of the proposed dynamic latch comparator is reduced.

2.6 The custom readout ASIC for photon counting and energy measurement

Photon-counting systems are based on the comparison of the charge generated by a single X-ray photon with a given threshold to determine whether this photon contributes to the output image or is discarded. Thus, each detected (counted) photon contributes with the same weight and the lowest measurable signal is a single photon. Since the threshold is set above the noise, the background is eliminated, and large acquisition times are allowed. The dynamic range is therefore limited by the capacity of the digital counter. Furthermore, using multiple threshold levels or sweeping this threshold in consecutive acquisitions, information of the spectrum of the incoming X-ray photons can be obtained, at the expense of more complex Digital Pulse Processing (DPP) systems.

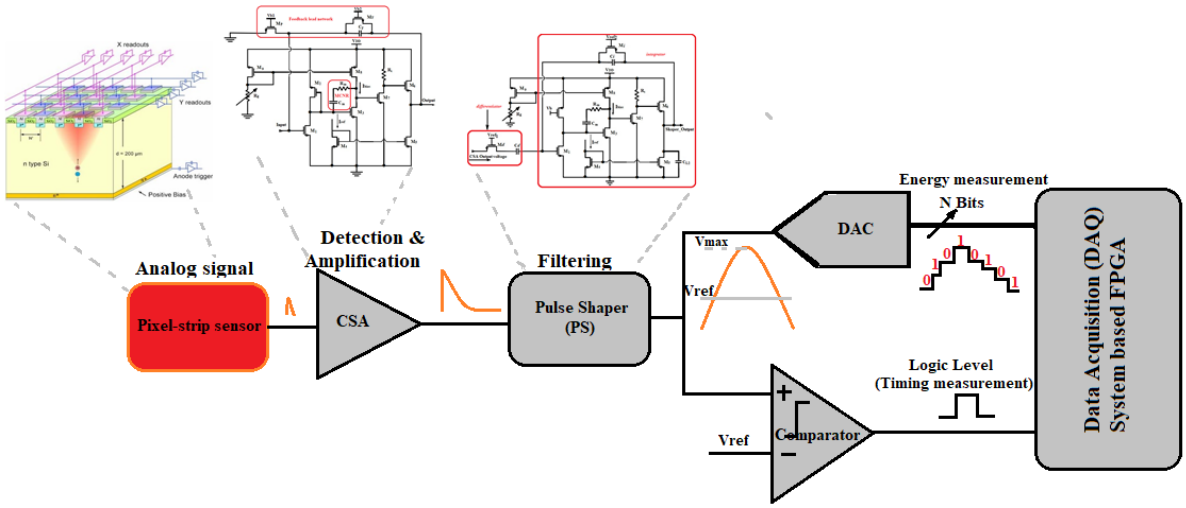


Figure.2.10: Block diagram of the proposed front-end ASIC chip for measuring the energy of a particle generated by a silicon detector.The CSA is used for extracting the charge at each strip and convert it into voltage.

The signal coming from the detector anodes is fed through the fast charge sensitive preamplifier. The preamplifier is based on Common source (CS) structure, which has been designed in the previous section. Thanks to CS based structure, the preamplifier has a

reasonably low input impedance (~100 Ohm) while maintaining a low quiescent current. These two characteristics are important for minimizing the crosstalk and static power consumption for multi-channel purpose. The pulse shaper (PS) is used to amplify and filter the voltage from the preamplifier thus giving a gain around 16.7 mV/fC. Afterward, the shaper output is sent to a voltage discriminator in order to transform this signal into trigger pulses. The threshold is used to discriminate the signal of the one channel front-end circuit. The output of the PS is processed into a digital format and sent to a data aquisition board based on field programmable gate array (FPGA).

2.7 Conclusion

Design methodology and techniques of a one channel readout ASIC for capacitive silicon detector applications have been described in this chapter. The ASIC is built of CSA, one-order Gaussian pulse shaper and a fast discriminator for generating the trigger signal. A fast analog to digital converter (ADC) module should be used to digitize signals coming from the complete ASIC and to reset the device. Since the amplitude of each pulse is proportional to the energy of the detected photon, it is then very important to measure it in order to obtain the energy spectrum from the histogram of all acquired amplitudes. This method of extracting information about the absorbed photons by mean of measuring peak amplitudes is often referred as Pulse Height Analysis (PHA). The ideal Digital Pulse Processing (DPP) chain for PHA should produce the most accurate and precise measurement of the analog (CSA or PS) output voltage step; independently of any constant offset and background constant slope with the highest noise attenuation first, secondly within the shortest period of time to efficiently deal with high photon rates (for pile-up rejection) and finally, optimizing the peaking time of the shaper which helps in improving the signal-to-noise ratio (SNR). Taking into account the above mentioned requirements and, in order to design an optimal and power-efficient ASIC, it is necessary to know all the relevant characteristics of the input signal. In our case, the input signal is the output of a capacitive semiconductor detector (Silicon strip or other small capacitive Si-based type detector). The FEE should be specially designed to deal with single photon detection systems. Based on this design methodology, our custom one channel ASIC was simulated, discussed and validated in the next chapter.

Chapter3

RESULTS AND DISCUSSION

3.1 Introduction

This chapter is devoted to the discussion of the main results obtained after simulating the different block designed in chapter 2 first, and validate the design through post layout simulation and process voltage and temperature (PVT) analysis. These results follow those of chapter 2 where the ASIC was analysed and designed in a CMOS technology. In section 3.2, the simulation results of the CSA and Shaper modules are presented and discussed. Noise optimization results are presented and discussed in section 3.3. In section 3.4, the fast discriminator based dynamic latch comparator is simulated and discussed. The design technique used to achieve very high speed circuit is well discussed. The global FEE-ASIC has been validated by post layout simulation and PVT analysis in section 3.5. The chapter is concluded in section 3.6.

3.2 Charge extraction and shaping: Front-End ASIC outcomes for pile-up cancellation in the High-Luminosity LHC

The Compact Muon Solenoid (CMS) experiment at CERN is foreseen to receive a substantial upgrade of the outer tracker detector and its front-end readout electronics, requiring higher granularity and readout bandwidth to handle the large number of pileup events in the High-Luminosity LHC [106]-[108]. The wide bandwidth purpose in the proposed design is achieved by controlling the gain stage in the CSA circuit by and external resistor, which allows providing a typical biasing current in the stage.

3.2.1 Simulation of the Loop gain.

In contrast to the spectroscopy amplifier, the most important factor for fast amplifiers is preservation of the fast rise time of the signal which means maintaining a wide bandwidth

[**109**].The open-loop gain (OLG) and the closed-loop gain (CLG) of the topology presented in Fig.2.2 were simulated for different biasing current and typical value of the input device parameters. Fig.3.1 shows the simulation results of the OLG versus frequency for differents biasing current.

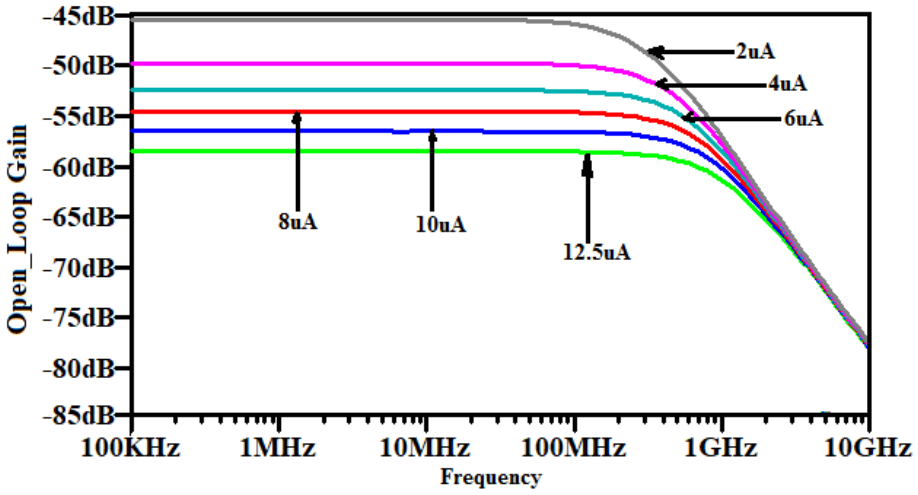


Fig.3.1 Open-loop gain of the proposed CSA for different bias current. It is controlled by the Ibias value for a feedback loop of R_F= 150 kΩ and C_F= 2 pF, W=42.5 µm, L=0.35 µm, C_L= 1 pF.

This configuration provided a bias current of 12.5 µA at the top level design. Frequency analysis swept from 1 Hz to 10 GHz and is displayed in decade form. The gain (absolute value) varied from 40.6 dB to 53.8 dB. The highest bandwidth of the amplifier is achieved by increasing the bias current till 12.5 µA, and is equals to 1.023 GHz. The optimization of the bias current in the second stage is very important to stabilize the bandwidth product and then maintains signal integrity [110].

However, a lower bandwidth solution can be achieved by reducing the load capacitance in this design. As depicted on Fig.3.2, the reduction of the load capacitance leads to reducing the loop gain therefore.

For frequencies lower than 100 kHz, the parasitic capacitance of the input transistor and the resistive feedback affect the gain of the CSA, thus its bandwidth. The closed loop bandwidth achieved in this topology is 459.6 MHz. The circuit is immune to those parasitic for frequencies greater than 100 kHz. The capacitor of the detector was set to 1 pF and the

parasitic capacitor of the input transistor is around 20 fF. So the total input capacitor was being fixed to 1.02 pF. It is important to remember that the negative gain is due to the internal feedback resistor created by transistors M6 and M7 in Fig.2.2.

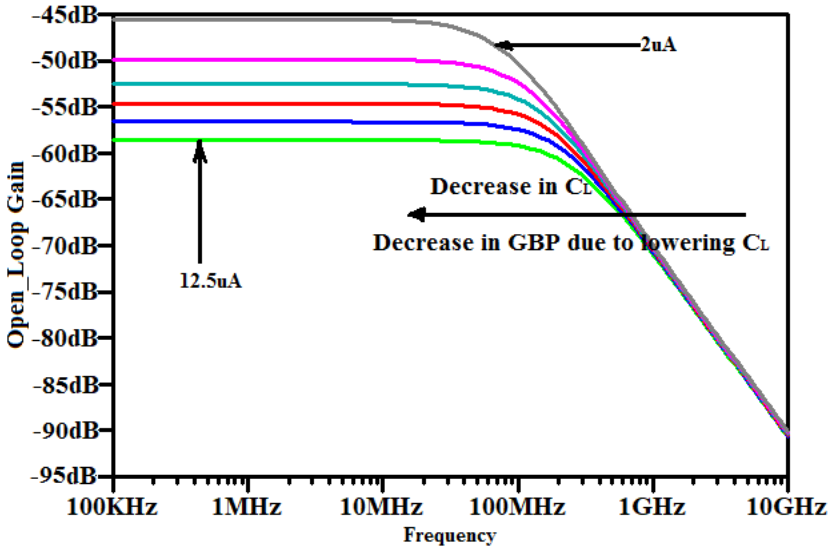


Fig.3.2: Lower load capacitance effects on the Open-loop gain of the proposed CSA for different bias current

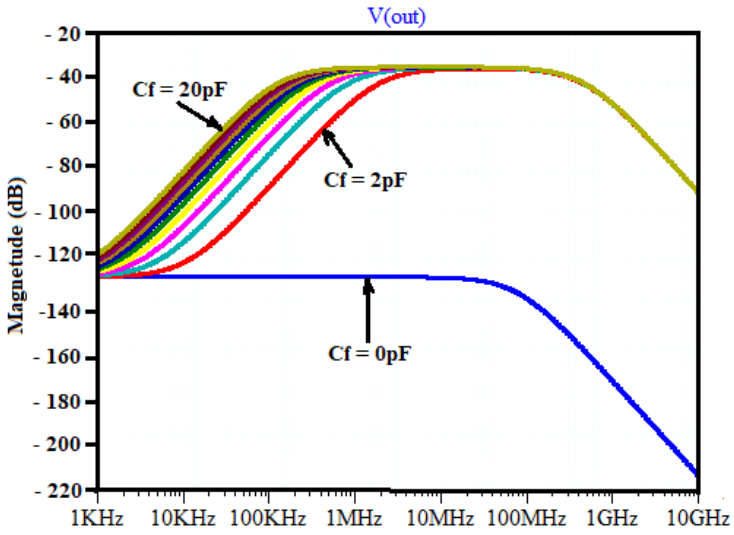


Fig.3.3 Closed loop gain simulation for different values of the load capacitance.

3.2.2 Transient simulation and circuit limitation: offset voltage and peak pileup effect

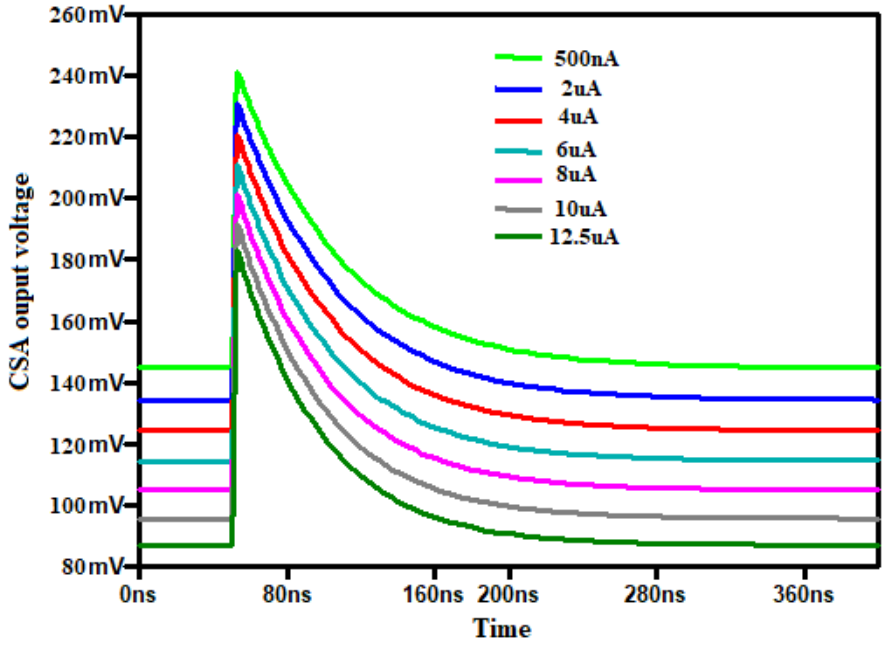


Fig.3.4: Transient simulation of the CSA output voltage showing the offset exhibited by the circuit for different biasing current. The design parameters were chosen as R_F= 150 kΩ and C_F= 2 pF, W=42.5 µm, L=0.35 µm, C_L= 1 pF.

As observed in Fig.3.5, the most important source of energy loss in this circuit is the pile-up effect. The peak pile-up occurs when two pulses are succinctly close together that they are treated as a same pulse by the analysis system. The resulting pulse has a height that is a combination of the two pulses. This type of pile-up leads to a distortion in the recorded spectrum; it also disturbs quantitative measurements based on measuring the area under the pulse. Because peak pile-up leads to the recording of one pulse instead of two, the total area under the recorded spectrum is also smaller than the total number of pulses presented to the system during its live time. The peak pile-ups create a continuous spectrum up to a double of the pulse heights, where the effect is most intense. This effectexacerbates at high count rate events.

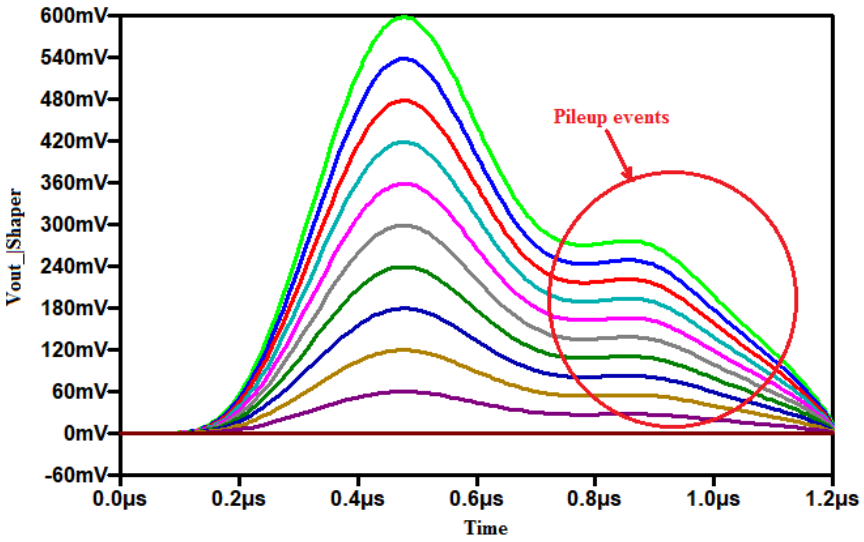


Fig.3.5: *Transient simulation of the Shaper output voltage showing the pileup effect for different bias current. The design parameters were chosen as* R_F= 150 kΩ and C_F= 2 pF, W=42.5 µm, L=0.35 µm, C_L= 1 pF.

3.2.3. Bandwidth compensation and pileup cancellation: Analysis and implementation of the analog FE-ASIC

Due to internal feedback issue and the failure of the bias current to maintain a constant and lower dc-offset, the topology presented in Fig.2.2 worsens the GBW of the CSA. To solve the problem, Fig.2.2 was modified and a new CSA topology was adopted in Fig.2.3**,** based on its small signal analysis model depicted on Fig.2.4, equations (2.8) to (2.13) have been derived and the open loop gain (OLG) of the modelled circuit has been computed for several design parameters. For the purpose, a MATLAB based toolkit has been developed in order to simplify the design [108]. The script in the toolkit uses small-signal parameters of the transistors and the parasitic capacitances as input data to assist in designing the three-stage opamps.

Fig.3.6 illustrates the frequency response of a Miller compensation nulling resistor (MCNR) three-stage Opamp designed for 42° phase-margin (black line). It is evident that the amplifier exhibited two poles; the dominant pole ω_{po}, the large pole ω_{p1} and one zero, all associated to equation (2.10). The poles are located at 74.6 kHz and 141.42 MHz respectively; and the zero is situated at the frequency of 998 MHz. The feedback network is designed to introduce a

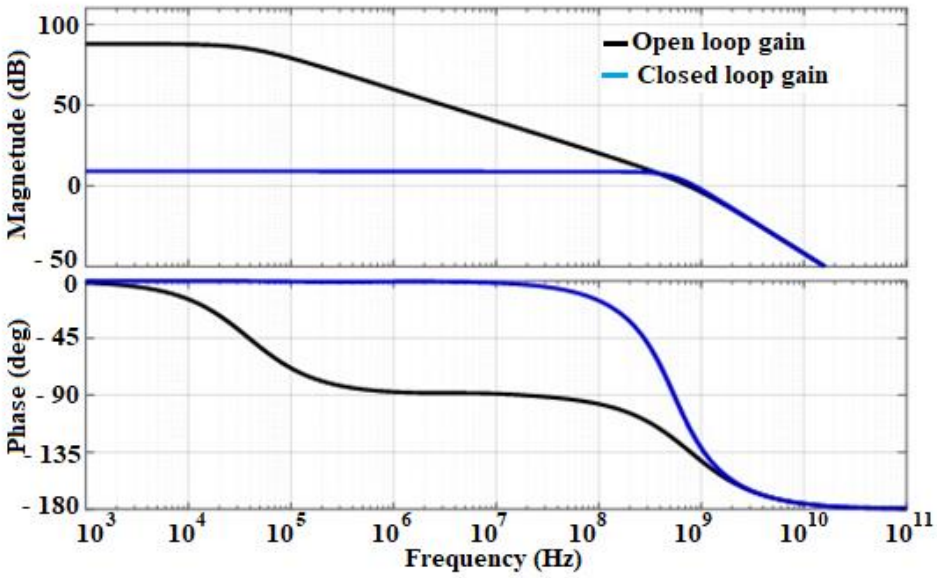


Figure.3.6. *Graphical demonstration of the OLG and CLG of third-order system with single pole dominant pole for* $C_3 \cong C_L = 0.1\ pF$ *and* C_m , C_L>>C_1,C_2,$C_m = 50$ fF

phase lead near the crossover frequency, thus cancelling the second pole of the Open-loop gain (OLG) which is located at the frequency of 141.42 MHz; then, increases the amplifier's phase margin.

The transfer function associated to the feedback network is well written in equation (2.13). The Open-loop transfer function (OLTF) and Closed-loop transfer function (CLTF) associated respectively to the Open-loop gain (OLG) and Closed-loop gain (CLG), the circuit of Fig.2.4 has been designed to fit the requirements of the theoretical analysis highlighted by equations (2.8) to (2.13). Therefore, rigorous transistor sizing and design should be implemeted in order to achieve better performance, taking in account the parasitic effects and mismatch that generate noise in the device.

The Spice simulation of the Open-loop transfer function (OLTF) and Closed-loop transfer function (CLTF) associated respectively to the Open-loop gain (OLG) and Closed-loop gain (CLG), are presented. The circuit should be designed to fit the requirements of this analysis. Therefore, rigorous transistor sizing and design should be implemeted in order to achieve better performance, taking into account the parasitic effect and mismatch that generate noise in the device.

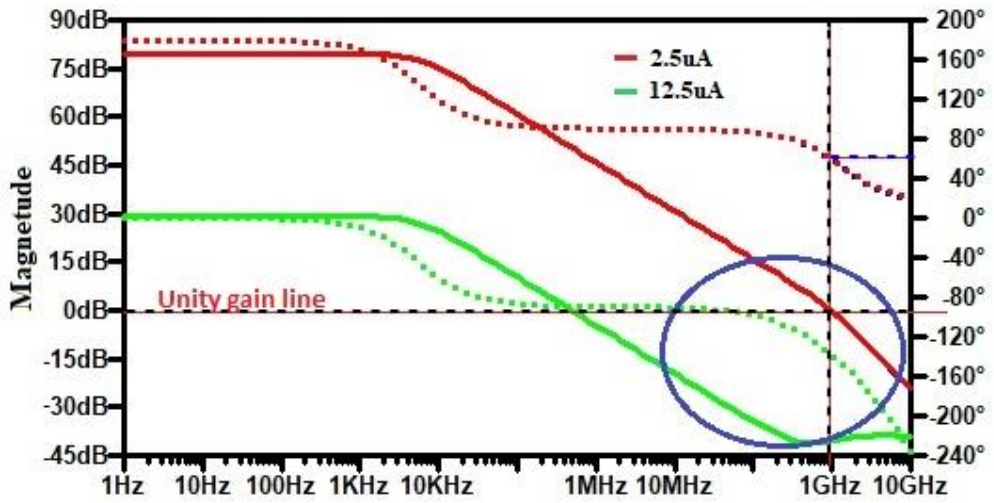


Figure.3.7. *Spice simulation of the OLG and CLG of third-order system for* $C_3 \cong C_L = 0.1\ pF$ *and* C_m , C_L>>C_1,C_2,$C_m = 50$ fF

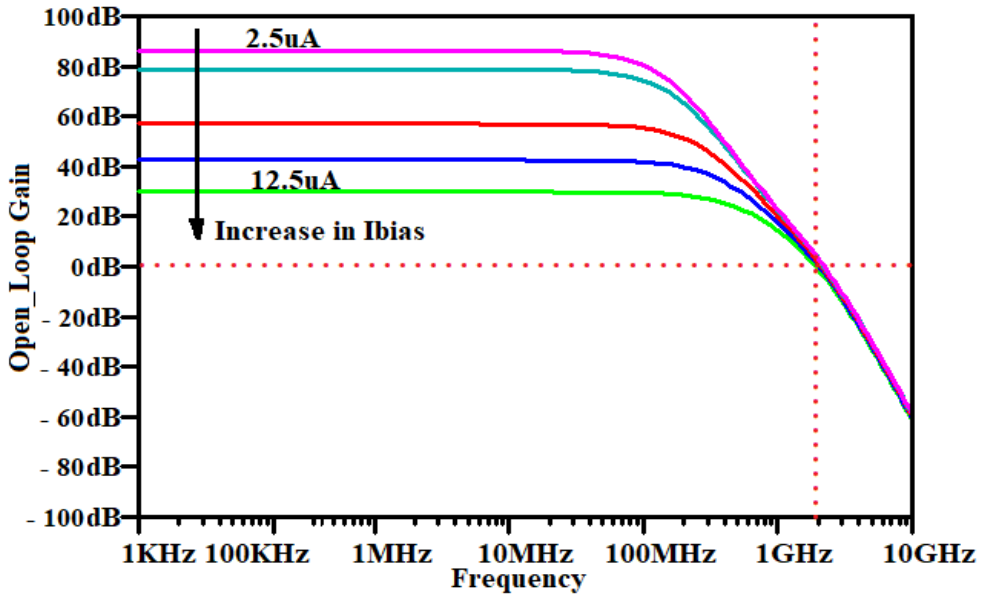


Figure.3.8: *Spice simulation of the open-loop gain for* I_{bias} *= 2.5 µA, of* I_{bias} *on the Open-loop gain showing the effect of the biasing current on the OLG*

Fig.3.8, shows the Spice simulation results of the open-loop gain (OLG) of the Opamp versus the I_{bias} current. It is evident that for low value of I_{bias}, wide GBW are achieved but involve a poor stability of the circuit. The simulated results show that the core amplifier achieved for 2.5 µA bias current, a unity gain-bandwidth of 997.84 MHz with 42° phase margin. The very

littledifference with the analytical value is due to the parasitic and the residual noise generated by the circuit. However, the phase margin remains poor and the circuit behaves unstable. Therefore, the bias current is a crucial parameter that may guarantee high dc-gain, the stability of the circuit needs to be compensated. Since the GBW is stabilized through the dc-gain, it should be necessary to keep the highest possible phase margin for maintaining signal integrity [112]. Therefore, the closed-loop gain (CLG) stability of the design is determined by its feedback network. Since the detector capacitance was set to 2 pF and the extracted parasitic capacitor of the input transistor was around 20 fF; the total input capacitor was fixed to 2.02 pF. Nevertheless, a resistor has a parasitic capacitance and a capacitance has a parasitic resistance. Thus, an RC feedback network (R_F-C_F) models the feedback circuit. Loop-gain stability has been evaluated during the charge vs voltage conversion when R_F-C_F is bypassed [108]. The Opamp equivalent load capacitors are also taken into consideration by varying C_F. For achieving the highest stability of the circuit, the closed-loop gain is adjusted by the R_F-C_F sizing. The feedback equivalent resistor was implemented by associating the drain-source resistance of two N-channel MOSFETs (M_F and M_p on Fig. 3.2) device biased to be in the triode strong inversion region. Under this condition, the parallel noise was reduced to a great extent; the circuit behaves therefore stable and continuously sensitive and can be maintained in this condition without adjustment for spectroscopy purposes [108, 114, 115 and 116]. Thus, with that technique, we achieved up to 3.542 MΩ feedback equivalent resistances, which guarantee a phase margin of 82^o.

The closed-loop gain of the design is shown of Fig.3.9. As depicted on that plot, the maximum unity bandwidth (UBW) achieved by the design (for stability conditions) is controlled at 1 GHz, which is a bit different from the one obtained in the open loop condition. Thus, the feedback compensation circuit and the parasitic capacitance of the design produce and error estimated at 0.216 % on the GBW. The difference with the analytical model is just 0.016 %. This little difference is due to the fact that the analytical solution was computed with ideal components, neglecting therefore some internal capacitance and mismatch produced by

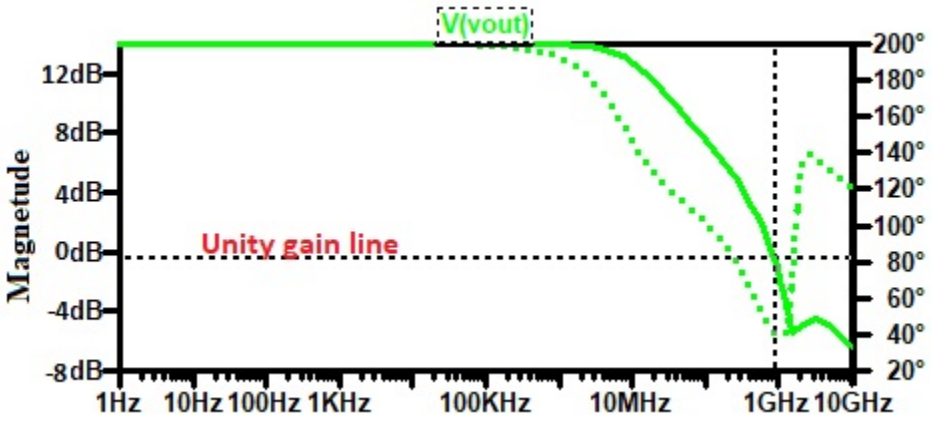


Figure.3.9: *Bandwidth compensation using a feedback lead network based MOSFET resistors; which allow achieving high stability.*

the devices. Adjusting I_{bias} as shown in Fig.3.7, enhances the phase margin and the bandwidth could be extended to more than 2 GHz for a target application. In fact, the compensation capacitor introduces a pole and zero into the loop equation. The zero always occurs before the pole because $R_F > R(M_F)||R(M_p)$. The zero is placed to cancel out the first pole along with its associated phase shift. The analytical closed loop transfer function shown in Fig.3.6 (blue line), was confirmed by the Spice simulation results in Fig.3.7. When the τ_F zero is placed at ω_{p1}, it cancels out the pole (p1) causing the Bode plot to continue on a slope of –20 dB/decade. When the frequency gets to $\omega_F = 1/R_F C_F$, this pole changes the slope to –40 dB/decade. The phase shift is completely canceled before the second op-amp pole occurs, and the circuit reacts as if the pole was never introduced. The benefit of pole zero cancellation is improved pulse shape and resolution in the energy at high counting rate [78, 109, 111].

3.2.4. Pulse shape simulation and energy monitoring of the FE-ASIC.

The LTSPICE transient simulation analyzes the timing performance for the designed analog front-end signal processing channel. The high counting rate simulation performed by rapid succession of the input current pulses (*Ipulse*) tests the shaper output response of the designed front-end ASIC.

a- Charge-to-voltage conversions

The transient analysis has been used to simulate the output response for the CSA and the Shaper from 0 to 400 ns. Corresponding to a radiation event taking place 50 ns with an input charge of 3 fC (Fig.3.10), the CSA and shaper output responses are presented in Fig.3.11 and Fig.3.12.

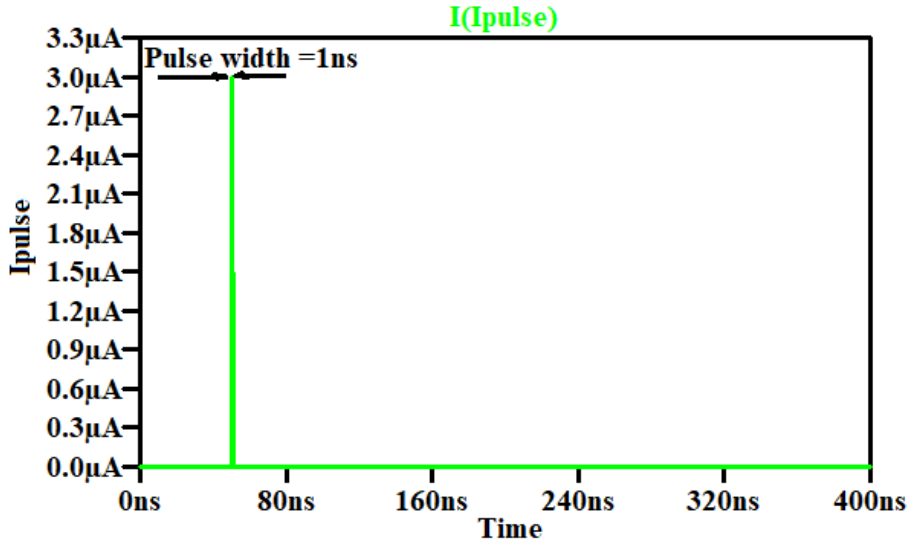


Fig.3.10. Injected input charge of 3 fC (3 µA with 1ns pulse width)

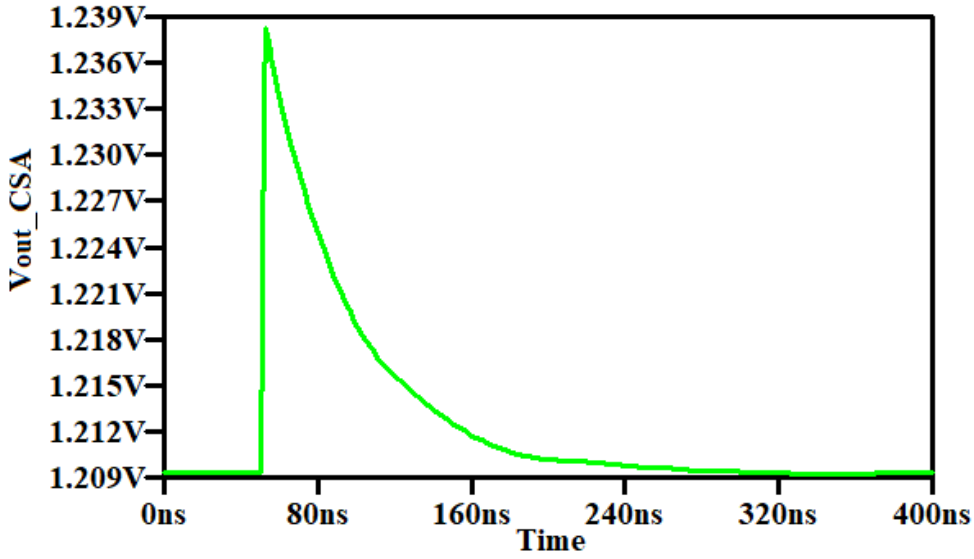


Fig.3.11. CSA output swing for 3 fC injected input charge

The achievablefast charge collection process, the rise time of the CSA circuit is derived as follow: $t_r = \frac{2.2}{2\pi GBW}$, where GBW is the gain bandwidth of the CSA core amplifier. From this formula, a fast pulse response of 7.36 ns was guaranteed for reaching 1 GHz bandwidth. In order to transfer quickly the charge generated by the detector, CSA, the GBW off the circuit core amplifier must be sufficiently large.

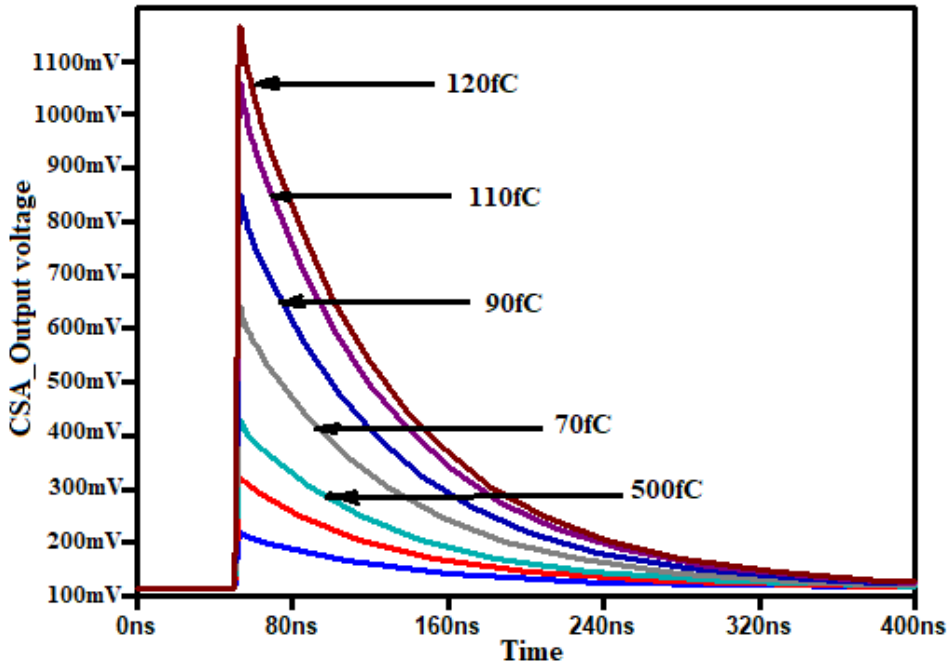


Figure.3.12: Shaper output swing for 3 fC input charge

b- **Offset voltage and pileup effect at the CSA output.**

Let us consider a simple CSA with a feedback capacitance C_F and a parallel feedback resistance C_F to discharge $C_F$capacitor and to avoid amplifier saturation. The CSA response to a negative δ-like current pulse carrying charge $-Q_{in}$ can be written as

$$V_{out,CSA}(t) = \frac{Q_{in}}{C_F} exp\left(-\frac{t}{\tau_F}\right) \quad (3.1)$$

where $\tau_F = C_F R_F$.

The train of input pulses of high average frequency f_{in}generates a "positive" DC voltage shift $V_{Shift,CSA}(t)$ at the CSA output (pile-up on pulse tail), which can be calculated as [113]

$$V_{Shift,CSA}(t) = f_{in} \int_0^{\infty} V_{out,CSA}(t)\, dt \quad (3.2)$$

Using the formula (3.1) and assuming that all the input pulses carry the same charge $-Q_{in}$, the equation (3.2) can be rewritten as

$$V_{Shift,CSA}(t) = Q_{in} f_{in} R_F \quad (3.3)$$

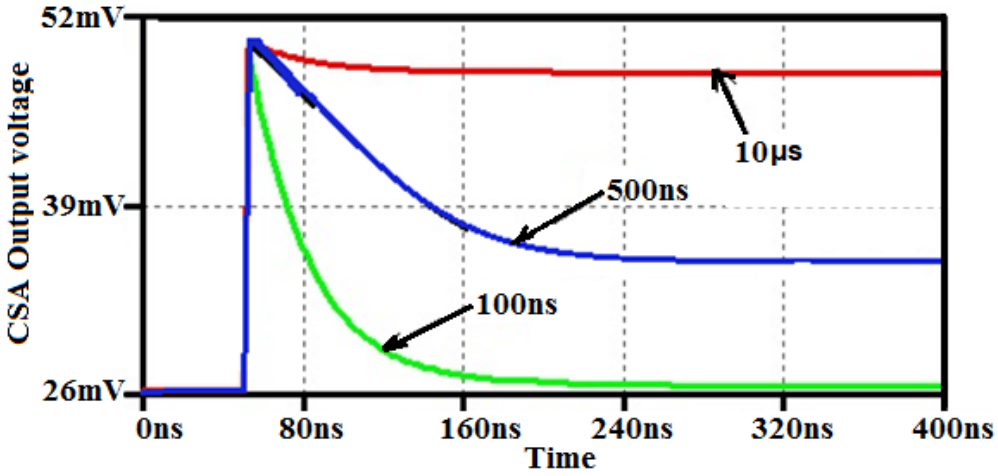


Fig.3.13. Pulses for different CSA feedback time constant at the CSA output

It is clear that the DC voltage shift $V_{Shift,CSA}(t)$is proportional to the charge *Qin* of the input pulse, the average frequency f_{in} and to the feedback resistance R_F. A compromise should be found for the $R_F$value in order to obtain an acceptable $V_{Shift,CSA}(t)$without significant deterioration of circuit noise.

c- Pole-zero cancellation circuit

When the feedback capacitor C_F is discharged with the effective resistance R_F, the CSA pulse output decays exponentially with a time constant $\tau_F = C_F R_F$. In most cases, the following stage is a semi-Gaussian pulse shaper consisting of one RC differentiator and *n* integrators with the same τ time constant. In most cases the condition $\tau << \tau_F$ is true. If CSA output pulse with a long tail is fed into a popular RC-$(CR)^1$ filter the answer at the shaper output is as follows:

$$V_{out,SH}(s) = \frac{Q_{in}}{C_F} \frac{1}{s+\frac{1}{C_F R_F}} \frac{s}{s+\frac{1}{CR}} \left(\frac{1}{sCR+1}\right) \quad (3.4)$$

In the time domain the above pulse has a long "negative" undershoot, whose amplitude and width depend on the time constant τ_F and its relation to filter time constant τ - see Fig.3.14

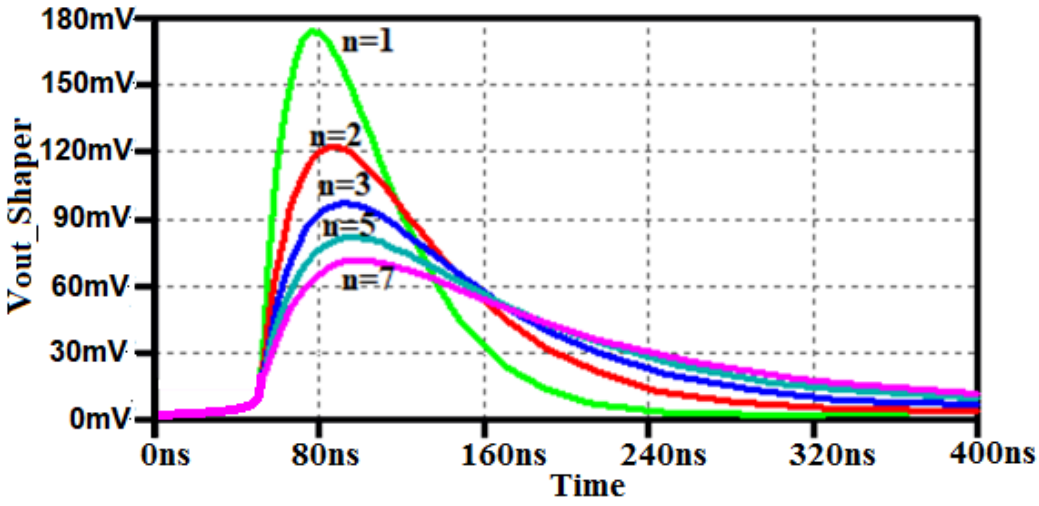


Fig.3.14. Pulses for different CSA feedback time constant at the shaper output the second order shaper with t_p=80 ns.

At low rates of input pulses, this pulse overshoot is usually tolerable; however, in high rate experiments the consecutive input pulses produce a negative baseline shift at the shaper output and loss of the amplitude resolution of the system (see Fig. 3.15). Additionally, if the readout system operates at high fluctuating random rates, a significant base line variation is produced. The undershoots can be eliminated (see Fig.3.16) by applying the pole-zero cancellation circuit [80].

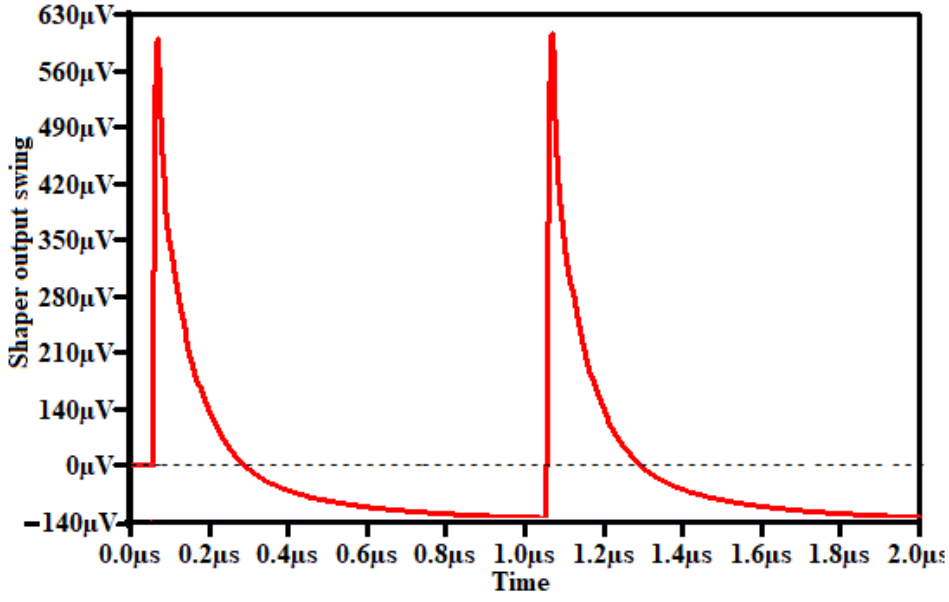


Figure.3.15: Output voltage of the CSA for high rate input without Pole Zero Canceller (PZC) circuit

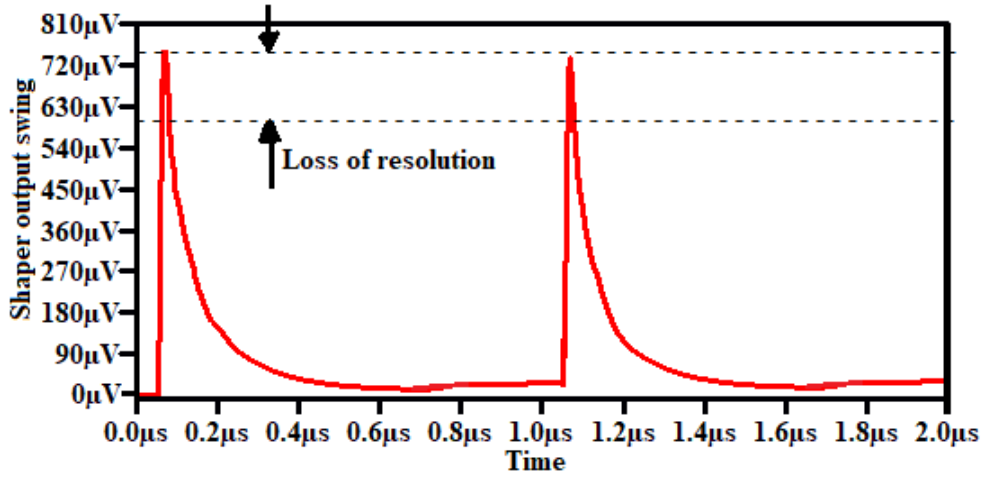


Figure.3.16: Output voltage of the CSA for high rate input with the PZC circuit.

The idea of a PZC circuit is shown in Fig.3.17. By adding an extra resistor *Rpz* (parallel to capacitor *C*) the long-time constant τ_F at CSA output can be cancelled by the subsequent stage if the following condition is fulfilled.

$$C_F R_F = C R_{pz} \tag{3.5}$$

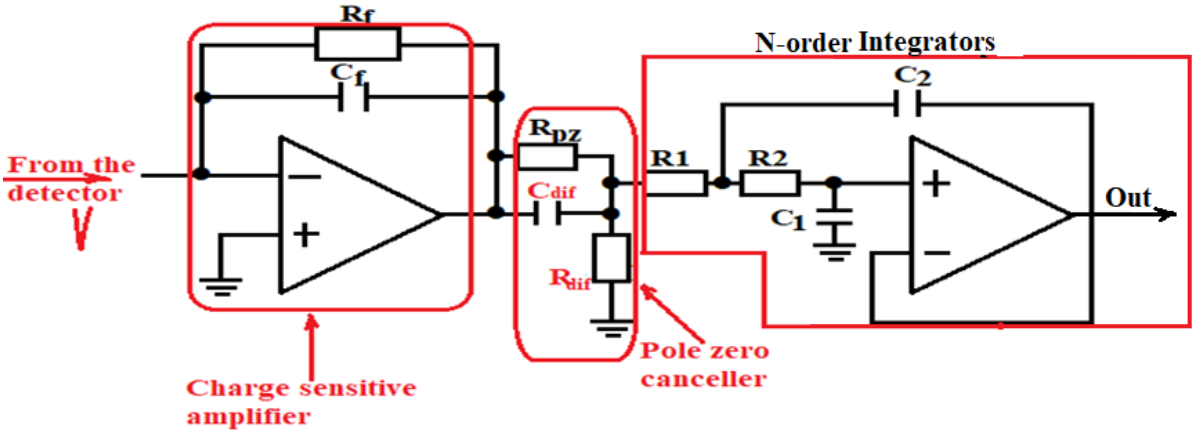


Fig.3.17. Pole Zero Canceller (PZC) circuit highlighted

Then the pulse at the shaper output is given by

$$V_{out,SH}(s) = \frac{Q_{in}}{C_F} \frac{1}{s+\frac{1}{C_F R_F}} \frac{s+\frac{1}{CR_{pz}}}{s+\frac{1}{C(R//R_{pz})}} \left(\frac{1}{sCR+1}\right) \tag{3.6}$$

Since, $C_F R_F = CR_{pz}$, the above equation can be rewritten as

$$V_{out,SH}(s) = \frac{Q_{in}}{C_F}\frac{s+\frac{1}{CR_{pz}}}{s+\frac{1}{C(R||R_{pz})}}\left(\frac{1}{sCR+1}\right) \quad (3.7)$$

The "pole" of the CSA is cancelled by the "zero" of the PZC circuit. The new time constant after the PZC is equal to $C(R||R_{pz})$ and it is smaller than τ.

d- Pulse shaping modelling and simulations

The most common pulse shaping method is to produce a pulse whose peak amplitude is proportional to the detected charge in the detector. Three basic parameters are involved in the transfer function of a Semi-Gaussian shaper, namely, the time constant τ the number *n* and the dc gain *A* of the integrators. The Opamp designed for the CSA module is also customised for the SG-shaper unit. A simple semi-Gaussian pulse shaper of type CR-(RC)^n, which consists of one CR differentiator and *n* integrators has been proposed to simulate n-order effects on the shaper output swing.

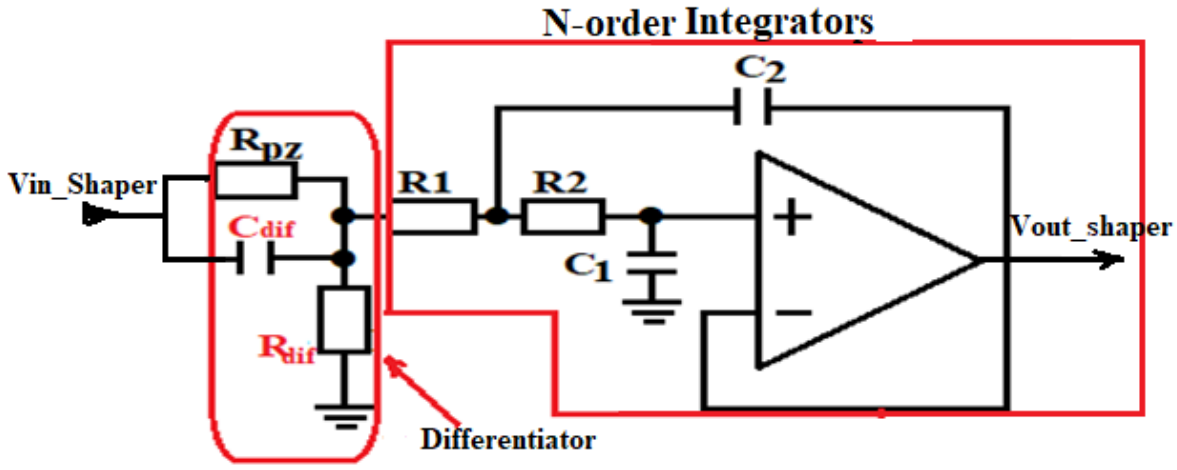


Fig.3.18 Semi-Gaussian pulse shaper of type CR-(RC)^n

For the CR-(RC)^n filter with the same integrator and differentiator time constants $\tau_i = \tau_d = \tau$ the transfer function is given by [77, 78].

$$H(s) = \frac{Q_{in}}{C_F}\left(\frac{s\tau}{1+s\tau}\right)\left(\frac{A}{1+s\tau}\right)^n \quad (3.8)$$

Assuming an ideal unity voltage step at the shaper input and taking the transfer function of the filter given by (3.9), one obtains the shaper output signal in the time domain as

$$V_{out,SH}(t) = \frac{Q_{in}}{C_F}\frac{A^n}{n!}\left(\frac{nt}{\tau_p}\right)^n exp\left(-\frac{nt}{\tau_p}\right) \quad (3.9)$$

The maximum peak amplitude of $V_{out,SH}(t)$ signal is given as:

$$V_{max,SH} = \frac{Q_{in}}{C_F}\frac{A^n}{n!e^n} \quad (3.10)$$

With$\tau_p = n\tau$ is the peaking time. The family of shaper output pulses for a given time constant τ is shown in Fig.3.19. Increasing the filter order results in decreasing the signal amplitude, but makes the pulse more symmetrical. Higher order filter is more suitable for high counting rate

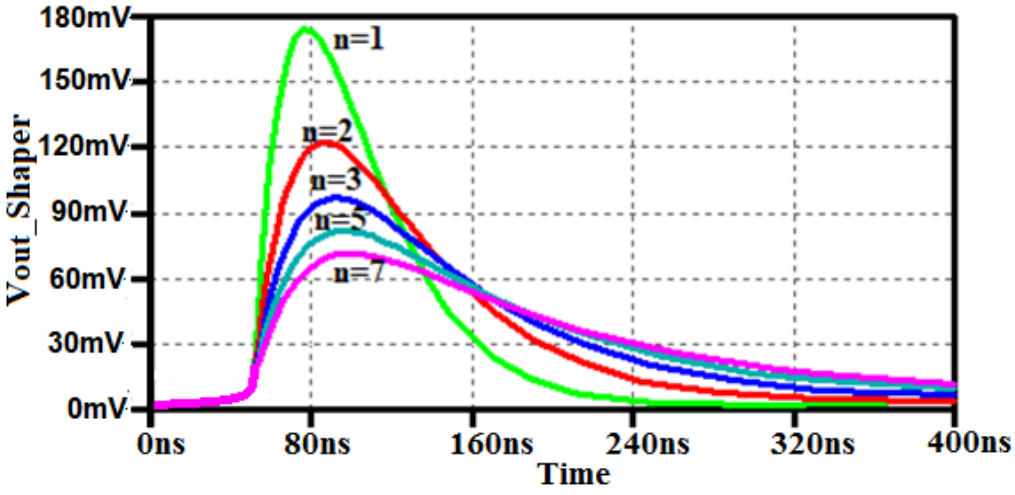


Figure.3.19. Family of shaper output pulses for a given time constant τ

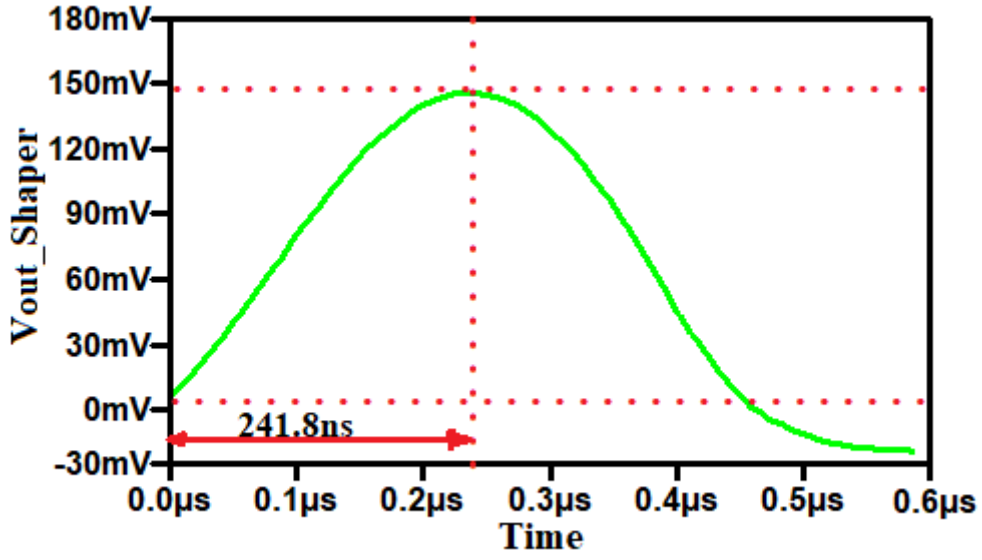


Figure.3.20. Shaper output swing for different input charge

applications, however to obtain the same peaking time for the higher shaper order, one should shorten the time constant of the filters. Therefore, we chose a first order pulse shaper circuit (Figure.2.5) which was designed to guarantee high count rate purpose by optimization of the shaping time and equivalent noise charge. The time responses of both the CSA and the pulse shaper circuit for different input charge have been simulated and given in Fig.3.20 and Fig.3.21 respectively.

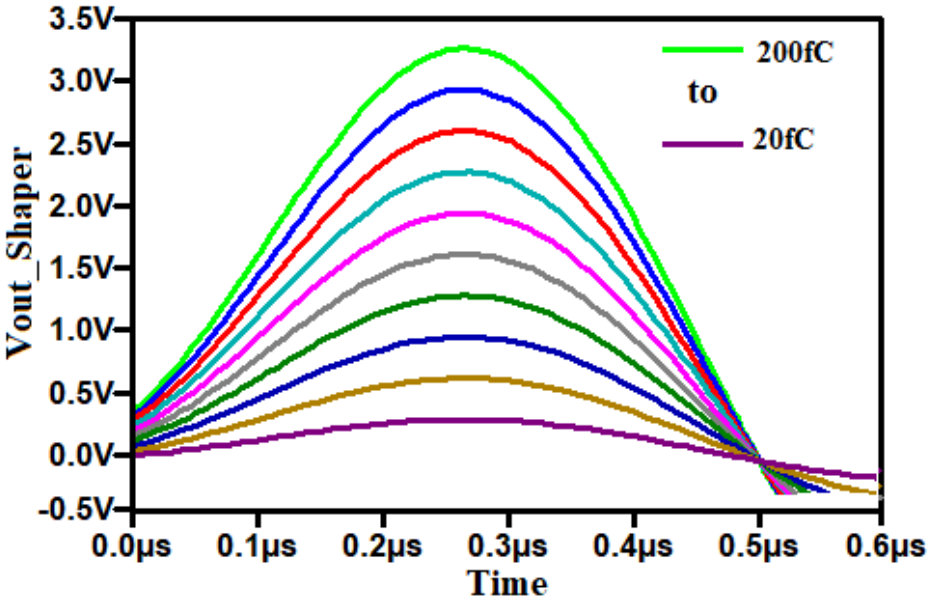


Figure.3.21: Shaper output swing for different input charge

The input charge dynamic range of the FEE is from 0 fC to 280 fC. The output voltage linearly increases with the increase of input charges, the charge-to-voltage gain from the output node of the CSA, the CR-RC shaper, is provided by simulation outcomes as, 546.56 mV/MeV (9.92 mV/fC) and 920.66 mV/MeV (16.7 mV/fC) respectively, using the equivalence from mV/fC to mV/MeV as mentioned in ref [42]. The output voltage range of the Shaper is 22 mV to -3.36 V. The overall gain of the readout module can be adjusted by the feedback capacitance of the CSA.

3.3. Noise behavior of the analog FEE circuit

The most common amplifier configuration in semiconductor detectors front-ends is the charge sensitive amplifier for its superior noise performance. The input-referred-noise (IRN) of the proposed CSA was simulated for frequency range of 600 MHz to 4 GHz as depicted on figure.3.22. The IRN spectral density extracted is 5.243 nV/√Hz. Furthermore, while designing recording analog front-end (AFE), a lower IRN ensures the signal quality of the recorded neuron activities and low power consumption will extend the lifetime of the implanted recording device in human body [107, 117]. However, in the CSA, the parameter that embodies the noise performance is the equivalent noise charge (ENC), namely the input charge necessary to get at the output a signal equal to noise. Its calculation was based on this intrinsic definition, neglecting the standard calculation depending on the post-CSA circuit, not present in this design [74]. Equations (2.21) and (2.22) were computed to provide optimal design parameters; an optimal shaping time of 214ns was theoretically extracted and the ENC_{total} was controlled at 37.35 e^- with for a detector capacitance of 0 pF and noise performance increases with a slope of 16.32 e^-/pF; while the Spice simulations provided a noise slope factor of 19.58 e^-/pF.

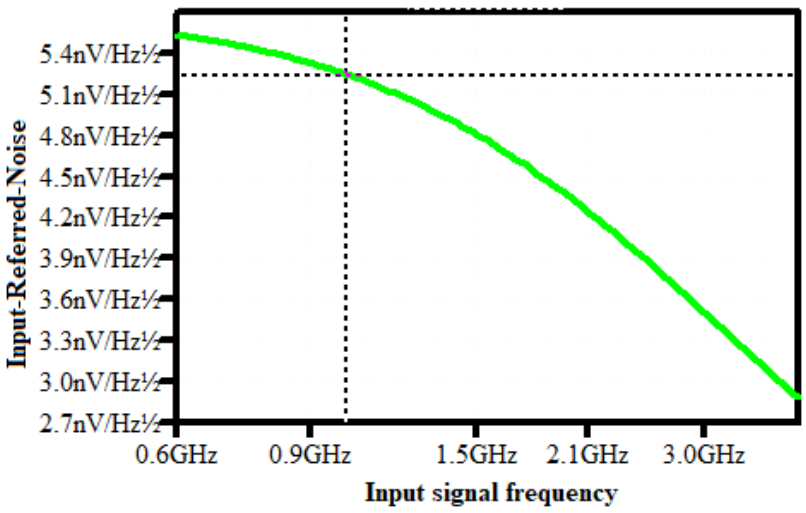


Figure.3.22. *CSA Input-Referred Noise.*

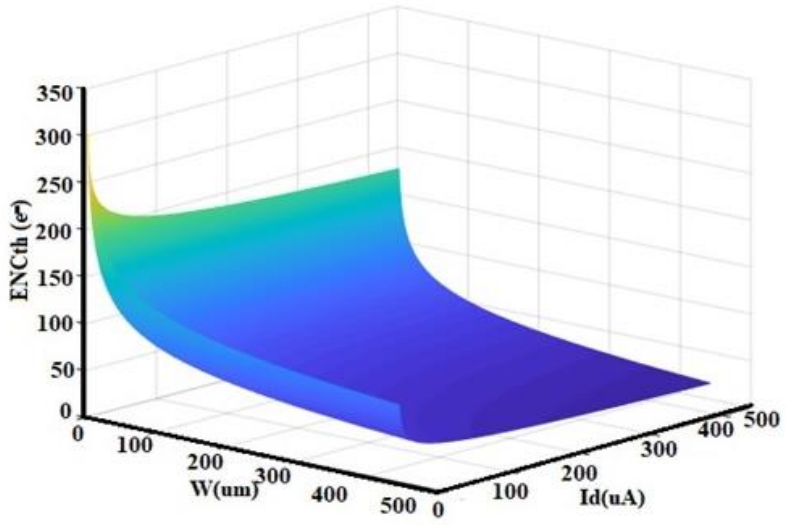


Figure.3.23. *ENC_{th} as a function of W and I_d.*

The equivalent noise charge as a function of I_D and W was computed and presented in Fig.3.23, while increasing the current in the input transistor, its thermal noise decreases but the bandwidth over which the thermal noise is integrated increases by the same amount; those effects cancelling each other out. Thus, if the device operates in a low count rate, environment substantial reductions in power consumption can be obtained with little or no noise penalty [118] by reducing the bias current of the input transistor provided a good separation between the preamplifier rise and fall time is ensured [119-122]. According to equation (2.22) we can note that, at short peaking times, the noise increases rapidly with capacitance and increases as the peaking time is reduced. For Si-PIN diodes, the capacitance scales with area, so large area detectors exhibit more noise. For Silicon Drift Detectors (SDD), the capacitance is much lower and nearly independent of area. This noise is only weakly dependent on temperature [115, 123]. At long peaking times, the noise decreases with peaking times (Fig.3.24 (d)) and increases with leakage current. Since leakage current increases exponentially with temperature, reducing temperature helps dramatically in lowering noise.

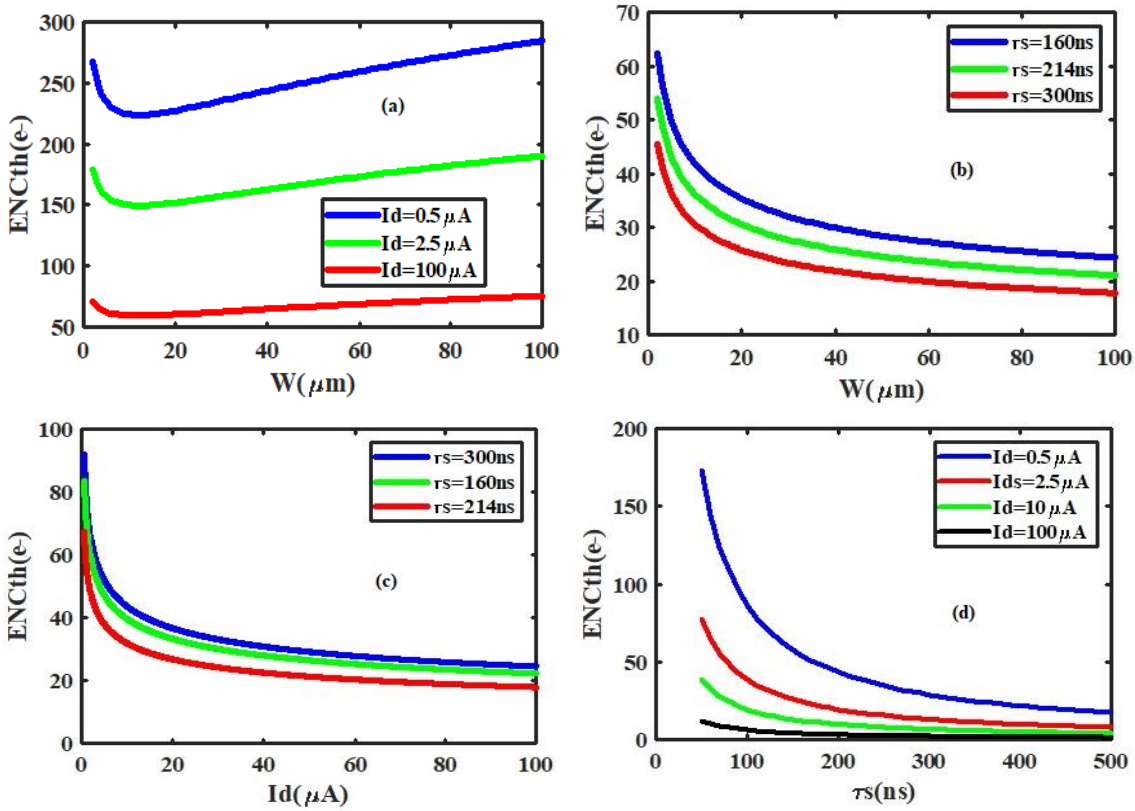


Figure.3.24. ENCth versus different design parameters: (a) as a function of W for different setting of the input device drain current; (b)as a function of W for different setting of the shaping time ; (c) as a function of the input device drain current for various peaking time; (d) versus the peaking time for different setting of the input transistor drain current.

As shown of Fig.3.24 (a, b, c and d), the design consideration staken to optimize the total ENC for the used technology are also used to choose the optimal Id and W as trade-off between ENCth specification of the peaking time and power consumption [75, 109, 124]. Those optimal parameters were Id=2.5 µA and Wopt=62.5 µm which corresponds to gm=61.4 µS. An optimal transistor channel length Lmin=10.5 µm was chosen to minimize the input capacitance of the CSA circuit therefore. Especially on Fig.3.24 (a and b) it is evident that ENC_{th} has a minimum value at Wopt, and that value has a low dependency on Id and τ_s respectively. From those two graphs, it is clear that above 62.5 µm, noise reduction with the drain current while increasing the peaking time is very low. The same observations prove that the dependency of the ENCth is very low above 2.5 µA (Fig.3.24.d). There will be always some peaking time at which noise is minimum, where the delta and step terms are equal.

There is no advantage for operating at a longer shaping time, because of the integration of more parallel noise during this period.

The optimum time constant is shorter for lower capacitance and longer for low leakage currents. Orthewise, the third term of equation (2.23) represents the shot noise (due to the leakage current of the detector) which could be considered to be 10 nA (for the worst silicon detector) while performing the total noise of the intrinsec CSA circuit (Fig.3.25).

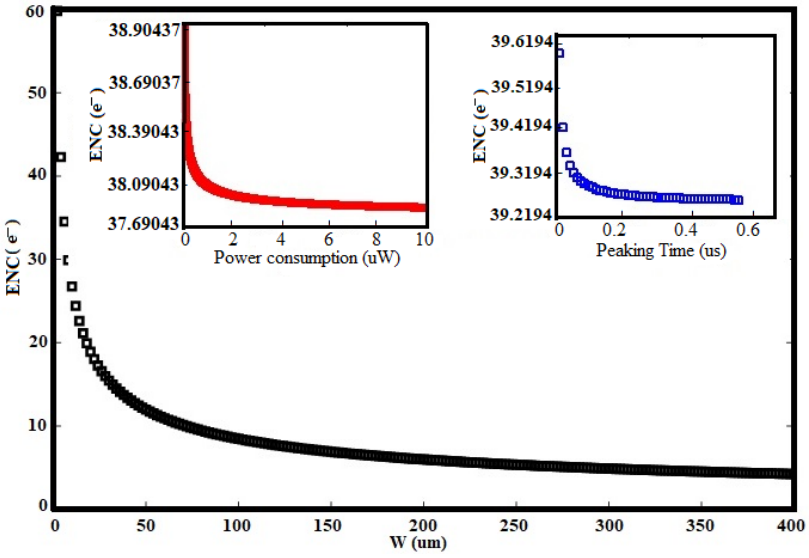


Figure.3.25a. $ENC_{1/f}$ as function of W (a)

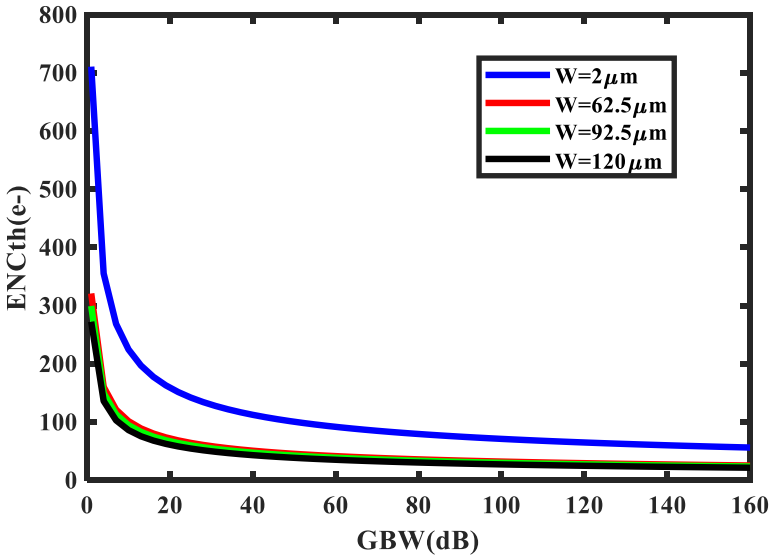


Figure.3.25bEffect of the CSA gain bandwidth (GBW) on ENC_{th} for several input gate width.

In fact, the intrinsec noise, represents the noise of the preamplier without any detector connected. The ENC varies from 38.90437 e^-r.m.s to 37.69043 e^- r.m.s as the peaking time is changed from 10 ns to 0.5 µs as shown on Fig.3.25 (a). The ENC is reduced when the power dissipation increases. The ENC achieves a value of 37.8632 e^-rms when the power dissipation is larger than 8.56 µW. This means that the specification of the power dissipation satisfies the design requirements.

Fig.3.25 (b) shows the effects of the CSA gain bandwidth on the ENC_{th}, with several input transistor width. It is readily recognized that lower transistor width leads to higher thermal noise for GBW from 1 to 20 dB. Since for lower GBW, the collection process is slowed down. Due to highest rise time, thermal noise accumulated in the device increases accordingly. This results in the attenuation of the output swing and therefore a poor energy resolution.

[75, 77 and 109]. As depicted on Fig.3.25, the optimal input transistor width (62.5 µm), is the critical value for which the variation of the thermal noise is not sensitive to the CSA gain

bandwidth. Therefore, from a point of view of minimizing the ENCth, a typical gate width is needed at a higher GBW [75, 109]. In a practical point of view, higher GBW leads to short rise time then very fast collection process. So, instead of the wide bandwidth of the CSA, the noise accumulation process is very brief due to the shortest collection time (7.36 ns). In this case, the optimal input noise matching conditions would result in optimal input transistor dimensions. Smallest transistor dimensions should be therefore taken at the expense of some system resolution [75, 77 and 109].

3.4 Pulse shape discrimination based fast dynamic latch comparator

3.4.1. Comparison speed enhancement and Offset reduction techniques.

In Fig.2.10, the NMOS load transistor's source swing from 0 to V_{DD} - V_{THN} when its gate and drain are clocked from 0 to V_{DD}; comparing to the PMOS counterpart in which nodes swing from 0 to V_{DD}. So, the differential output nodes (F1 and F2) should be pre-charged from 0 to V_{DD} - V_{THN} as shown on Fig.3.26. Furthermore, For NMOS, the V_{TH} is increased when its body-source voltage is biased to be negative. This is referred to as reverse body biasing (RBB) [95]. Besides, transistor M15 is sized so that its on-resistance allows the enhanced differential pair to be biased near the weak inversion at the start of the evaluation phase. When the clock is high (Clk=V_{DD}), the enhanced differential pair starts a specific tail current (*Icm*). The large finite resistance of M15 produces an increasing $\frac{g_m}{I_D}$ aspect ratio with decreasing $V_{GS.}$ The variability of V_{THP} and V_{THN} (in PMOS and NMOS transistors) tends to be quite high innanometer CMOS technologies [96].

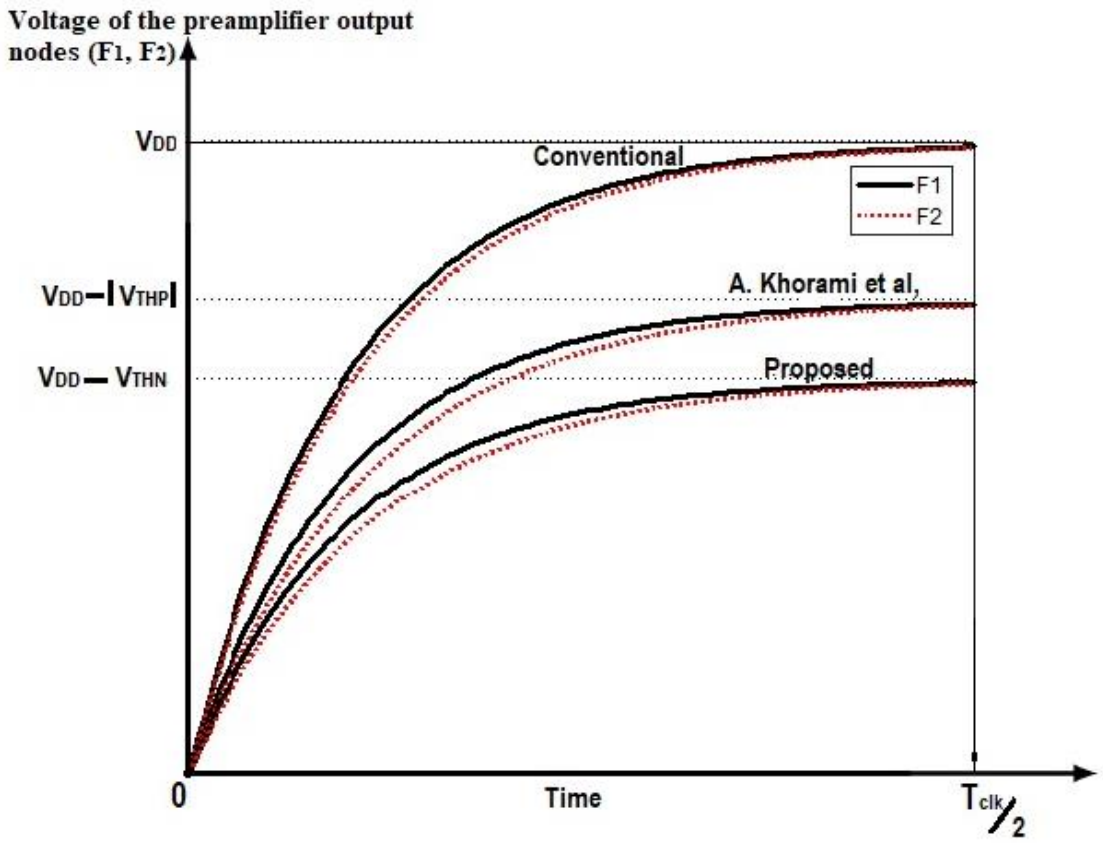


Figure.3.26. Voltage at the preamplifier output nodes during the evaluation phase for both the proposed, conventional and [21] topologies

As depicted on Fig.3.26, the comparison speed is much higher than that of the conventional one or the preamplifier of ref [97]. Moreover, low kickback noise is achieved due to using auxiliary transistors M5, M6, M7, and M8 in Fig.2.11 to isolate the preamplifier output nodes first, and secondly reducing mismatch effect and parasitic capacitance of the transistors while designing the devices. Transient simulations showing the outputs settling to inputs that are very close to the trip points of the latch circuit is given on Figure.3.27.

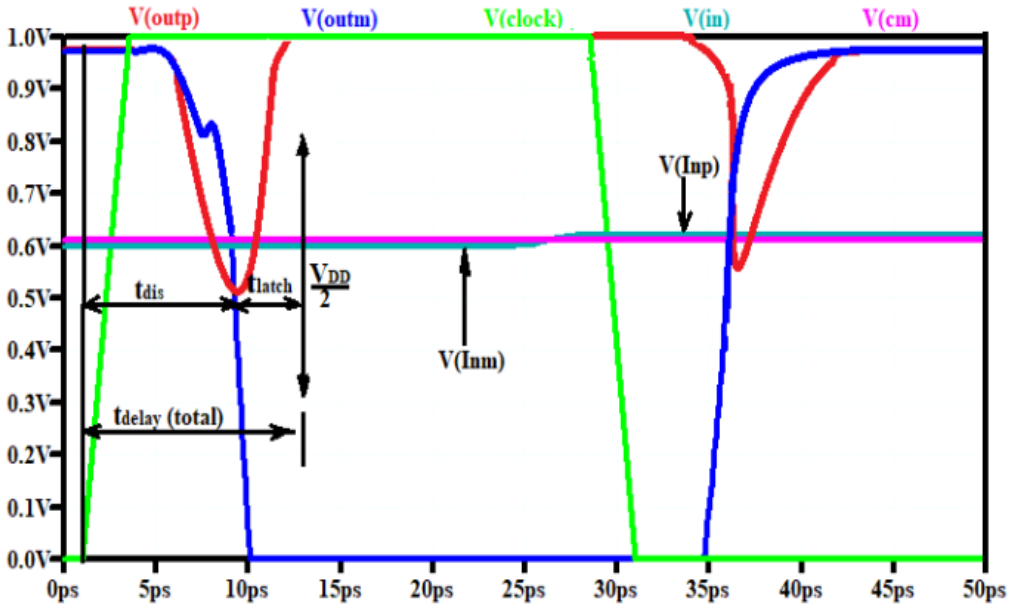


Figure.3.27. Transient simulation of the proposed dynamic latch comparator (VDD =1 V, Vcm=0.5 V, ΔVin = 5 mV, Clk= 20 GHz)

In fact, at the pre-charged phase, the input differential voltage is applied and amplified, while the regeneration process not yet started, no disturbance occurs [94]. At the beginning of the comparison phase, these auxiliary transistors are turned on and help the circuit to start the decision-making and then the regeneration process [103, 127]. Also, Those transistors which are in the triode region are parallel with input differential pair transistors and help in keeping the drain of the input transistors to sense a less voltage variation, which leads to less kickback noise [103, 128] as depicted on Figure.3.28. On that figure, the kickback noise error at the comparator outputs is simulated in the absence and the presence of M7, M8 devices and is compared to that produced by the conventional double tail comparator (CDTC) for 20mV differential input voltage (ΔVin=20 mV) during the reset-to-regeneration transition. The proposed comparator exhibited low kickback noise due to using the auxiliary transistors M7, and M8 to isolate the preamplifier output nodes first, and secondly reducing mismatch effect and the parasitic capacitance of the transistors while designing the devices. Therefore, the offset reduction in the feedback loop consisted of suitable transistor sizing operating in the weak inversion region and mismatch optimization [125, 129].

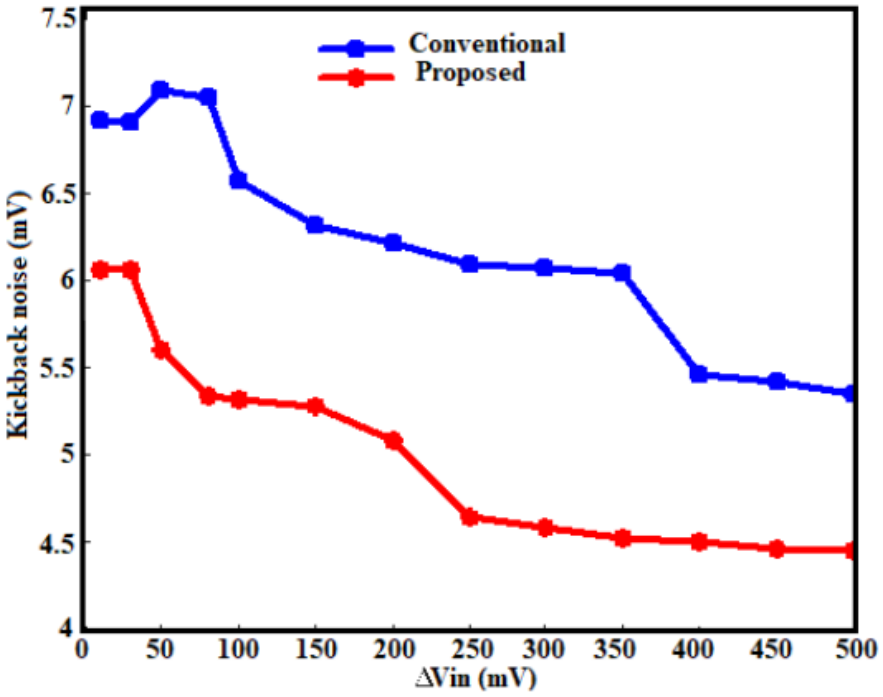


Figure.3.28a: Kickback noise error on the comparators output voltage versus differential input voltage

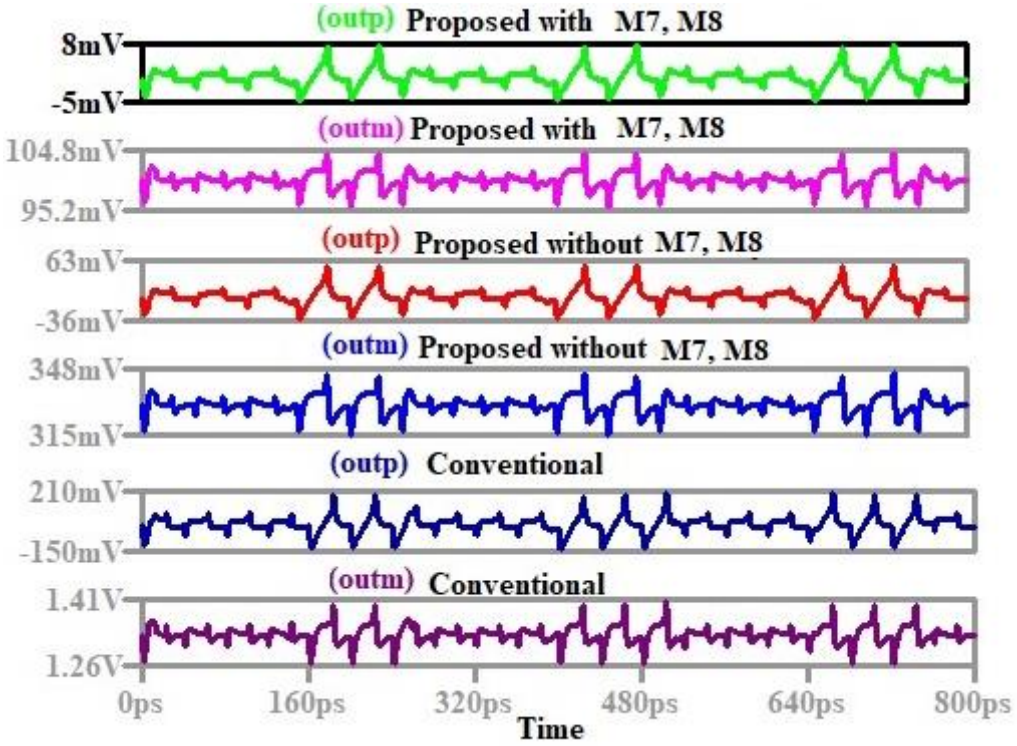


Fig.3.28b. Transient simulation showing the Kickback noise error at the Comparator Outputs for both the CDTC and the proposed circuit in the absence & presence of M7, M8 transistors

ΔVin = 20 mV

3.4.2. Delay and power optimization techniques

The design parameters of the proposed comparator were improved as compared to CDTC and comparators which have been proposed in ref [98] and refs [103, 129 and 130]. Figure.3.29 demonstrates the dependency of the proposed comparator delay on various differential input voltage levels at different supply voltages. For a given V_{DD}= 1 *V*, the delay is 35.6 ps at differential input voltage level ΔVin= 10 *mV*. This delay falls from 35.6 ps to 14.8 ps while ΔVinvaries from 10mV to 500 mV. Furthermore, at a particular ΔVin, the higher the supply voltage (V_{DD}), the higher the comparator delay will be. The worst-case delay of 35.6 ps for V_{DD}= 1 *V* for ΔVin= 10 *mV* and the best of 14.8 ps for V_{DD}=0.8 *V* and ΔVin= 500 *mV*; the common-mode voltage being set to 500 mV ($0.5V_{DD}$). The effect of the input common-mode voltage (*Vcm*) on the delay of the comparator was simulated for 500 mV differential input under different supply voltages, and the results are shown in Figure.3.30. When V_{DD}= 1 *V* and *Vcm*= 500 *mV*, the delay is found to be 47 ps. For a fixed value of V_{DD}, the delay decreases while the input common-mode voltage (*Vcm*) increases. As illustrated in Figure.3.30, the delay is sensitive to the input common-mode voltage. The worst-case delay of 47 ps is exhibited for *Vcm*= V_{DD}= 0.5 *V* and the best case of 14.4 ps was controlled for *Vcm*= V_{DD}= 1 *V*.

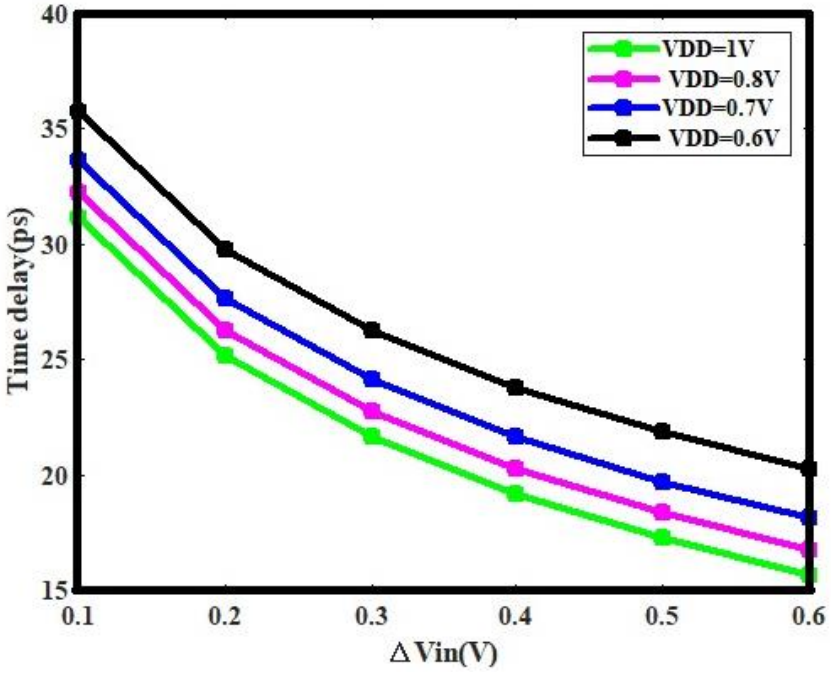


Figure.3.29. Delay of the proposed comparator versus differential input voltage (VDD =1 V, Vcm= 0.5 V , Clk= 20 GHz).

Figure.3.31 shows the simulated delay of the proposed comparator with different widths of switches M5,6. As illustrated in Figure.3.31, when the width of those switches is larger than 3 μm, increasing the width would not help to reduce significantly the delay. For instance, at a given ΔV_{in}= 10 mV, the delay drops from 77 ps to 13.8 ps, as width drops from 0.6 μm to 4 μm. The delay becomes almost constant for widths larger than 3.2 μm. In these considerations, the extracted value of the delay is found to be 13.8 ps.

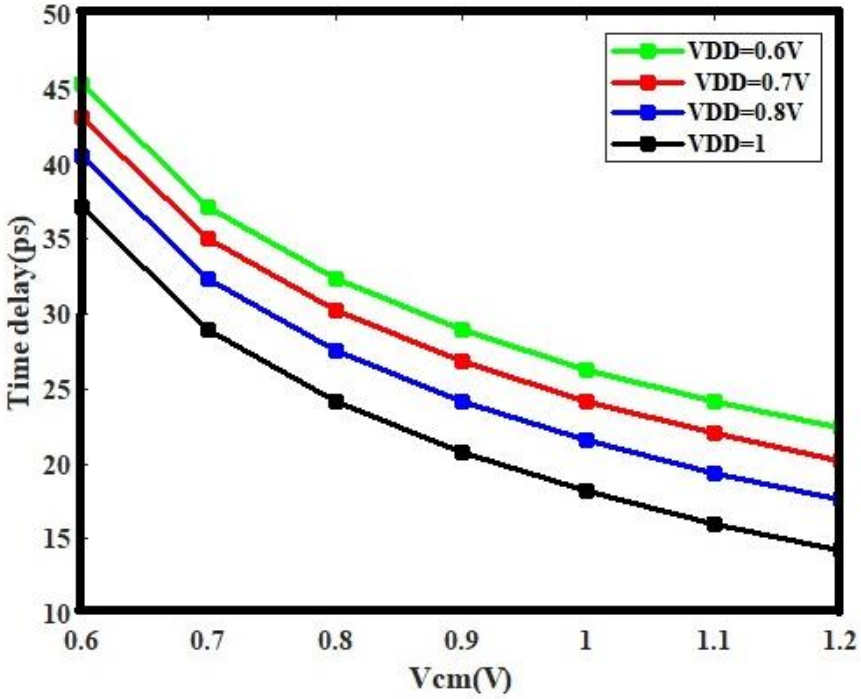


Figure.3.30. Delay of the proposed comparator versus input common-mode voltage (VDD = 1 V, ΔVin = 0.5 V, Clk= 20 GHz)

The spice simulation of the proposed comparator is illustrated in Figure.3.32, with 3.8 fF as extracted load capacitor at the Outm and Outp nodes of the latch. It is observed from Figure.3.32 that, with 1 V positive step for the input Vinp and keeping Vinm fixed to 0.5 V, *Vcm*= 0.5 *V* and Clk=20 GHz the proposed dynamic latch comparator can switch successfully. Voutp and Voutm are the latch's output voltage and Vout stands for the comparator's output voltage after filtering noise coming from the latch. In fact, the last stage of the comparator not discussed in this work, plays an important role in filtering the noise coming from the latch. Due to the hysteresis present in the output buffer, the output transition will take place only when the latch output is sufficiently high or low resulting in sharp, well-defined digital data.

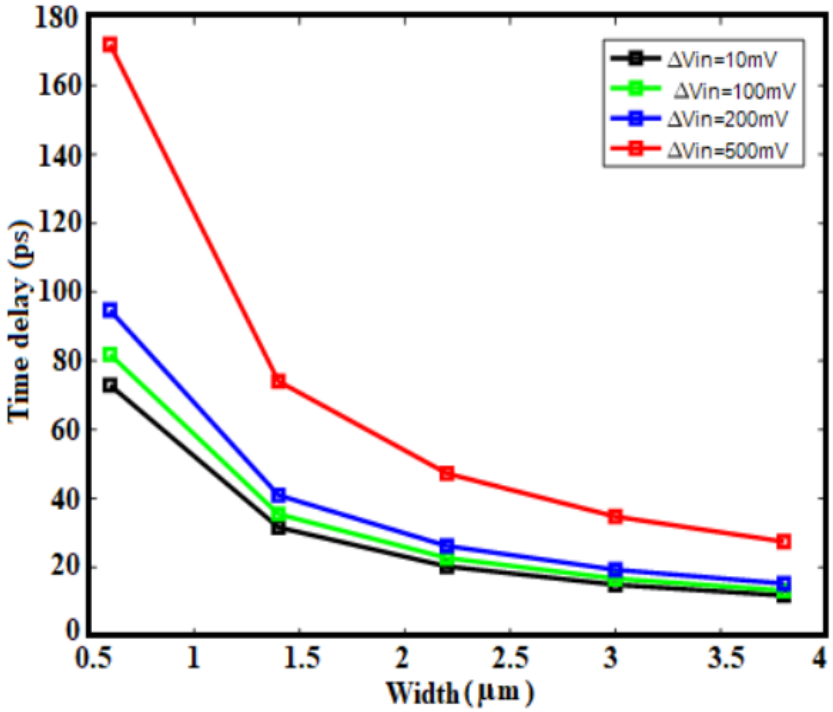


Figure.3.31. Delay of the proposed comparator versus the width of switches M5, M6.

3.4.3. Transient simulation of the dynamic latch comparator: Trigger level

The clock frequency being set to 20 GHz and the input signal frequency to 4 GHz. The voltage supply was 1 V with common mode input voltage of 0.5 V and 100 mV Δ*Vin*.

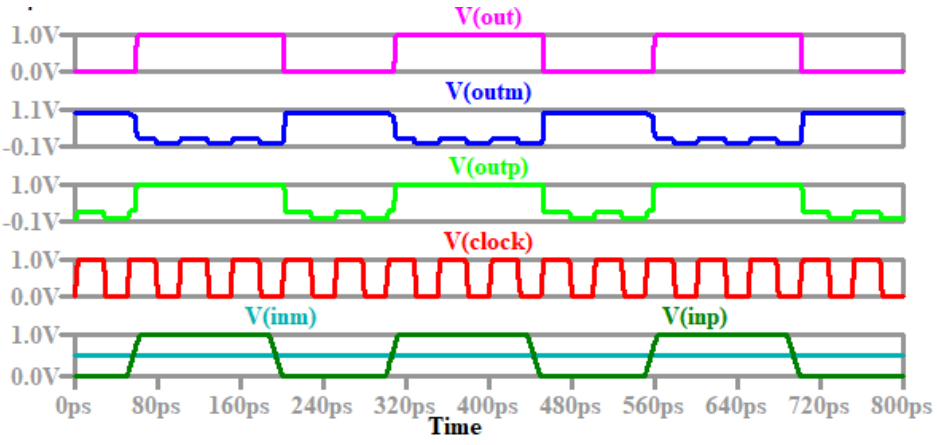


Figure.3.32. Spice simulation of the time response of the proposed dynamic latch comparator VDD = 1 V, Vcm= 0.5 V, ΔVin = 0.5 V, Clk= 20 GHz, Cout= 3.8 fF)

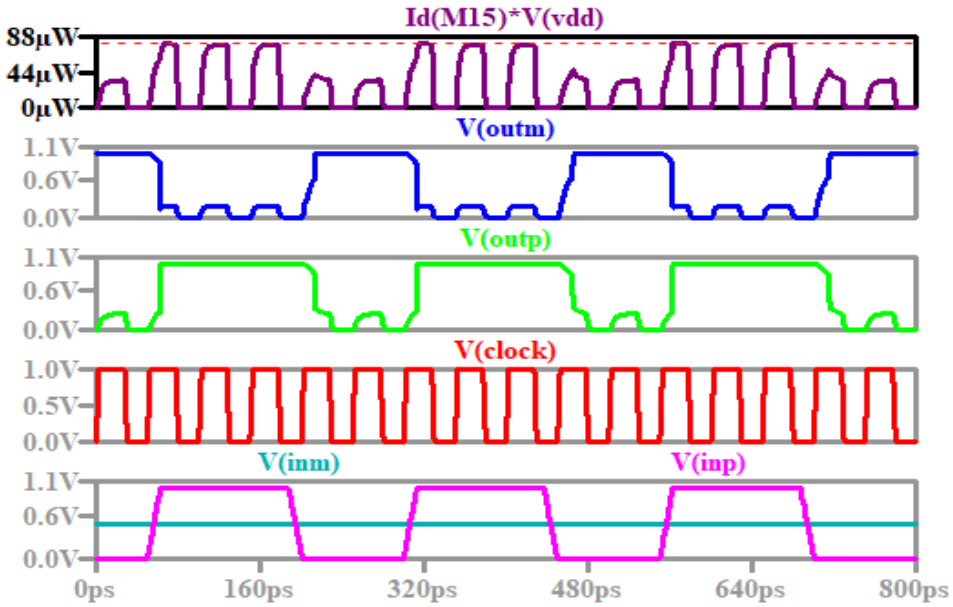


Figure.3.33. Spice simulation results for the average current of the proposed dynamic latch comparator from 1 V power supply.

Our design consumes a very low amount of current exhibited in Figure.3.33. Spice simulation results show that the comparator circuitry requires the only 67.8 μA, which is the average current for 20 GHz clock frequency. Moreover, the power dissipation of the design is 67.8 μW under 1V voltage supply.

3.5 Design validation and silicon implementation of the FE-ASIC

3.5.1. Post layout simulation of the amplification module.

Power-efficiency and robustness of the proposed circuit against process variation were performed through a post-layout Monte-Carlo simulation. As illustrated in Fig.3.34, this histogram describes the response function of the proposed FEE against several radiation events. This corresponds to the histogram of the energy of the detected particles (or injected charges) in real-time operations [67, 126 and 131]. Two important observations can be made. On the one hand, the output swing (offset voltage) for 0 fC is very low and is about 22 mV. This means that the proposed FEE does not exhibit high input offset. On the other hand, the proposed design is capable of handling up to 280 fC without losing the integrity of the signal (Preserving the information of interest). So, exhibited a wide input charge range. The mean

output swing of the design was controlled at 1412.17 mV with a 7.65 mV standard deviation. The full-width half-maximum (FWHM) was only 12.23 mV and contributed only at ~1.87% of the output swing. Since the circuit energy response is illustrated by Fig.3.34, the lowest percentage of the FWHM is satisfactory and confirms that the proposed FEE can handle high-energy resolution for spectroscopic applications.

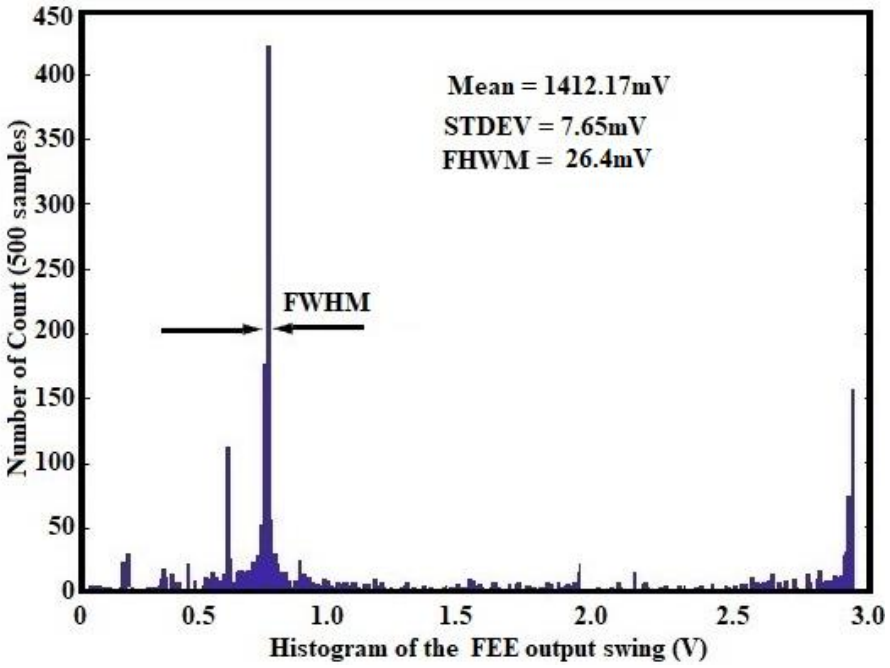


Figure.3.34. Histogram of output voltage for high charge production rate

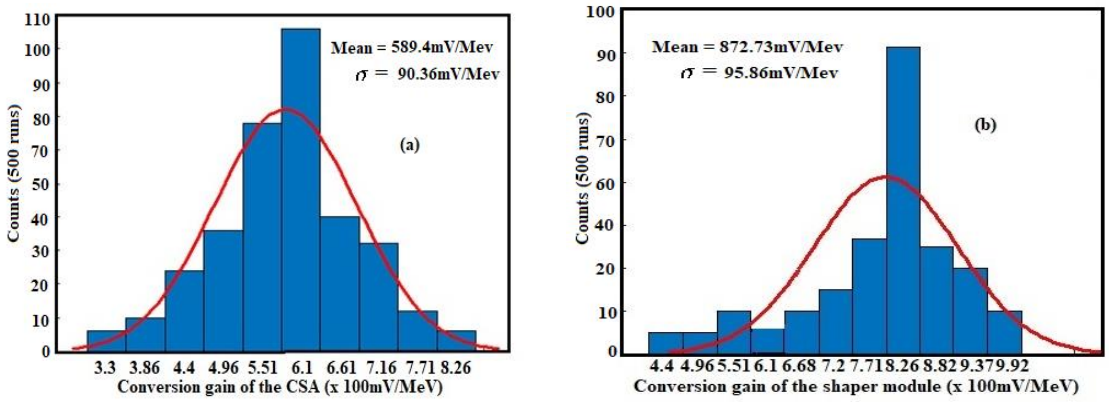


Figure.3.35. Histograms of the conversion gain for both (a) the CSA and (b)

Fig.3.35 shows the histograms of conversion gain based Monte-Carlo simulation results of the proposed front-end circuit for 500 runs, which exhibited the histogram of the conversion gain for both the CSA circuit and the PS module, for 10 fC charge injected at the input of the sensor. The highest sensitivity of the design is then achieved; for a week amount of injected

charge the histograms of the conversion gain observed on Fig.3.35 (a), (b) show a mean value of 589.4 mV/MeV, with a standard deviation of 90.36 mV/MeV for the CSA stage while the shaper circuit exhibited 872.73 mV/MeV mean value with 95.86 mV/MeV standard deviation. This shows that the outcomes got with Monte-Carlo models do not vary fundamentally for 500 runs and the front-end performance is very steady and robust. The less difference of those parameters with the spice simulation results is attributed to the parasitic capacitance obtained while designing the feedback circuits of the different stages. This can be compensated by adjusting the feedback capacitance of the CSA or increasing the loop gain of the shaper via an external device. Moreover, as highlighted in Fig.3.36, the ENC and shaping time are extracted from the post-layout simulation results and plotted for different values of power consumption. The system achieved an ENC of 37.6 e^- at 214 ns peaking time while dissipating only 8.72 µW of power from 3.3 V supply voltage. At 241.8 ns peaking time, the proposed front-end exhibited an ENC of 38 e^-, while consuming very less power of 10.14 µW. Those relatively low variations of equivalent noise charge and power consumption provided by the post-layout simulation at 241.8 ns peaking time do not differ to so much from those provided by the spice simulations; confirming, therefore, the ultra-low-power and low-noise behavior of our design.

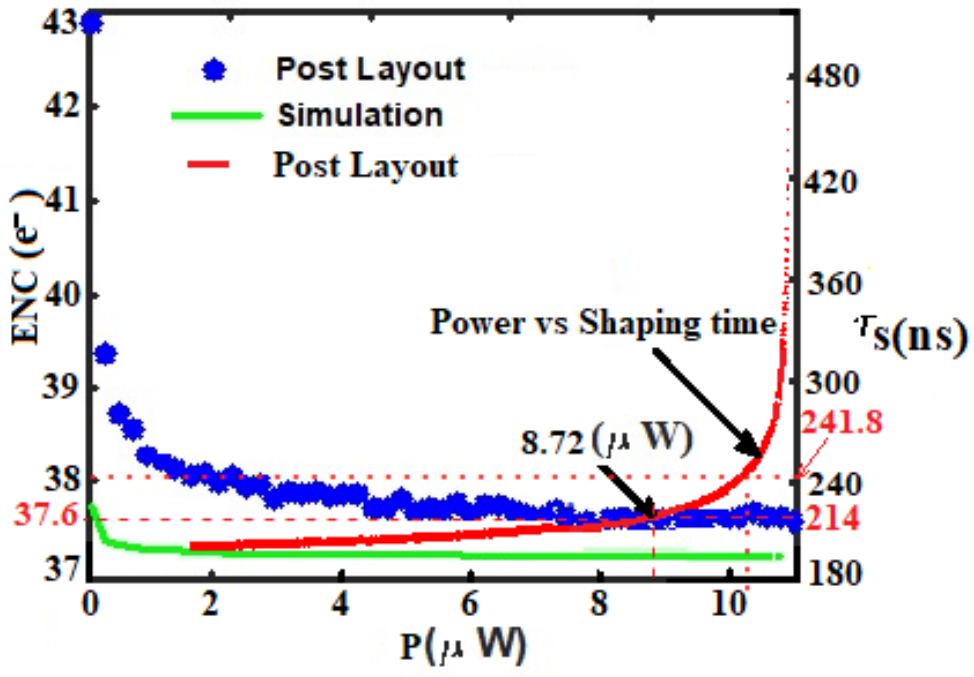


Figure.3.36. Validation of the design performance in terms of ENC, power consumption and shaping time.

3.5.2. Post layout simulation of the discrimination module

The mismatch and parasitic capacitance were reduced during the design process, using a parallel disposition of all the transistors of the circuits. The maximum operating frequency of the latch circuit is set by the propagation delay.

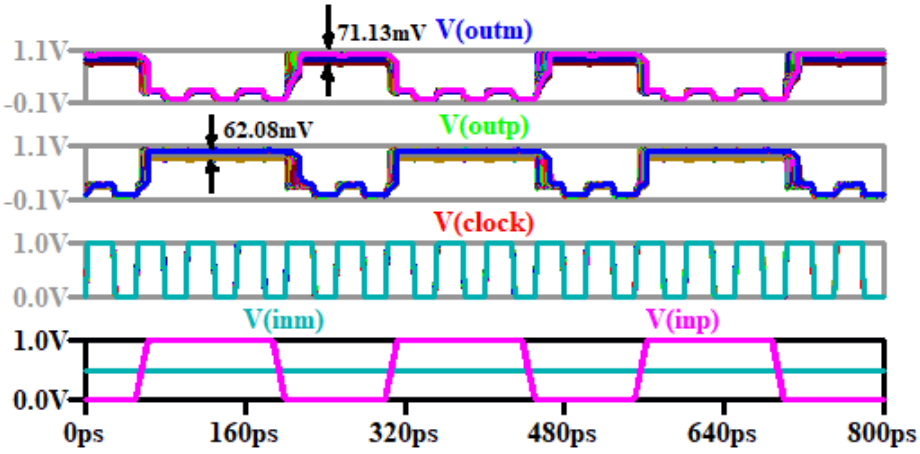


Fig.3.37. Post layout simulation of the time response of the proposed dynamic latch comparator VDD = 1 V, Vcm= 0.5 V, ΔVin = 0.5 V, Clk= 20 GHz, Cout= 3.8 fF).

Transient simulation provided by Monte-Carlo simulation outcomes is presented on Figure.3.37, which clearly reveals that at 20 GS/s sampling rate, the proposed DLC outputs swing do not vary significantly for 500 runs. It is evident that the error due to process variation on Voutp and Voutm are 62.0 8mV and 71.13 mV respectively. Therefore the latch outputs voltages vary from 0 to $V_{DD} - 62.08\,mV > \frac{V_{DD}}{2}$ (for Outp) and from 0 to $V_{DD} - 71.13\,mV > \frac{V_{DD}}{2}$ (for Outm) for 500 runs. This little variation does not affect the decision of the latch system; confirming therefore the 20 GHz clock frequency for high-speed operations.

The effect of the common-mode voltage, *Vcm*on power dissipation at various Δ*Vin* is simulated and the results are presented in Figure.3.38. It can be seen that power dissipation decreases with increase in *Vcm*from 0.5 V to 0.9 V, at particular Δ*Vin*. However, for *Vcm*swing from 0.9 V to 1V, power dissipation increases but remains lower comparing to it previous amplitude. For Δ*Vin* = 10 *mV*, the power dissipation is reduced from 81 μW at *Vcm*= 0.5 *V* to 38 μW at *Vcm*= 1 *V*. In general as depicted in Figure.3.38, the proposed comparator has less dependency on the *Vcm* due to the absence of the static and short circuit power dissipation.

Moreover, the post-layout Monte-Carlo simulation results for the offset voltage and time delay was performed to verify the reliability and the robustness of the design as depicted in Figure.3.39 (a) and (b) for 500 runs, respectively when ΔVin = 0.5 *V*, *Vcm*= 0.5 *V* and the clock frequency being set to 20 GHz while using 1V supply voltage. As shown on those plots, the average offset voltage of the circuit was controlled at 4.45 mV, while the standard deviation was 3.74 mV. Moreover, the average delay of the proposed design was only 14.28ps while the delay standard deviation was controlled at 1.82 ps. By the way, the effects of the internal capacitances of the MOS devices are taken into account through the extracted parasitic. That affects the output voltage of the latch circuit, involving kickback noise rather than affecting the speed of the device.

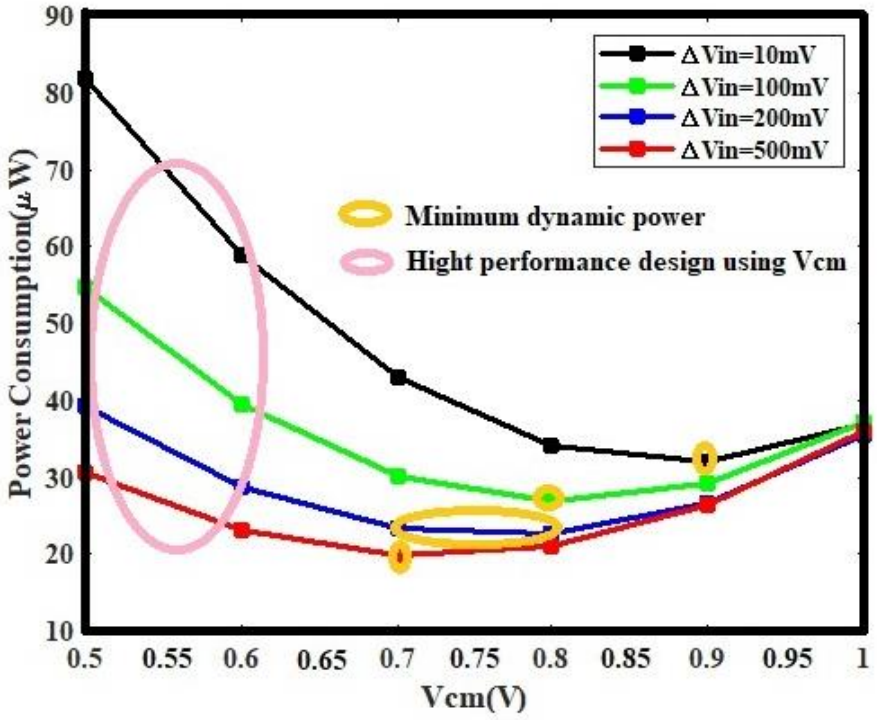


Figure.3.38. Simulation results of the power consumption versus input common-mode voltage, at various ΔVin, (Clk = 20 GHz and VDD = 1 V)

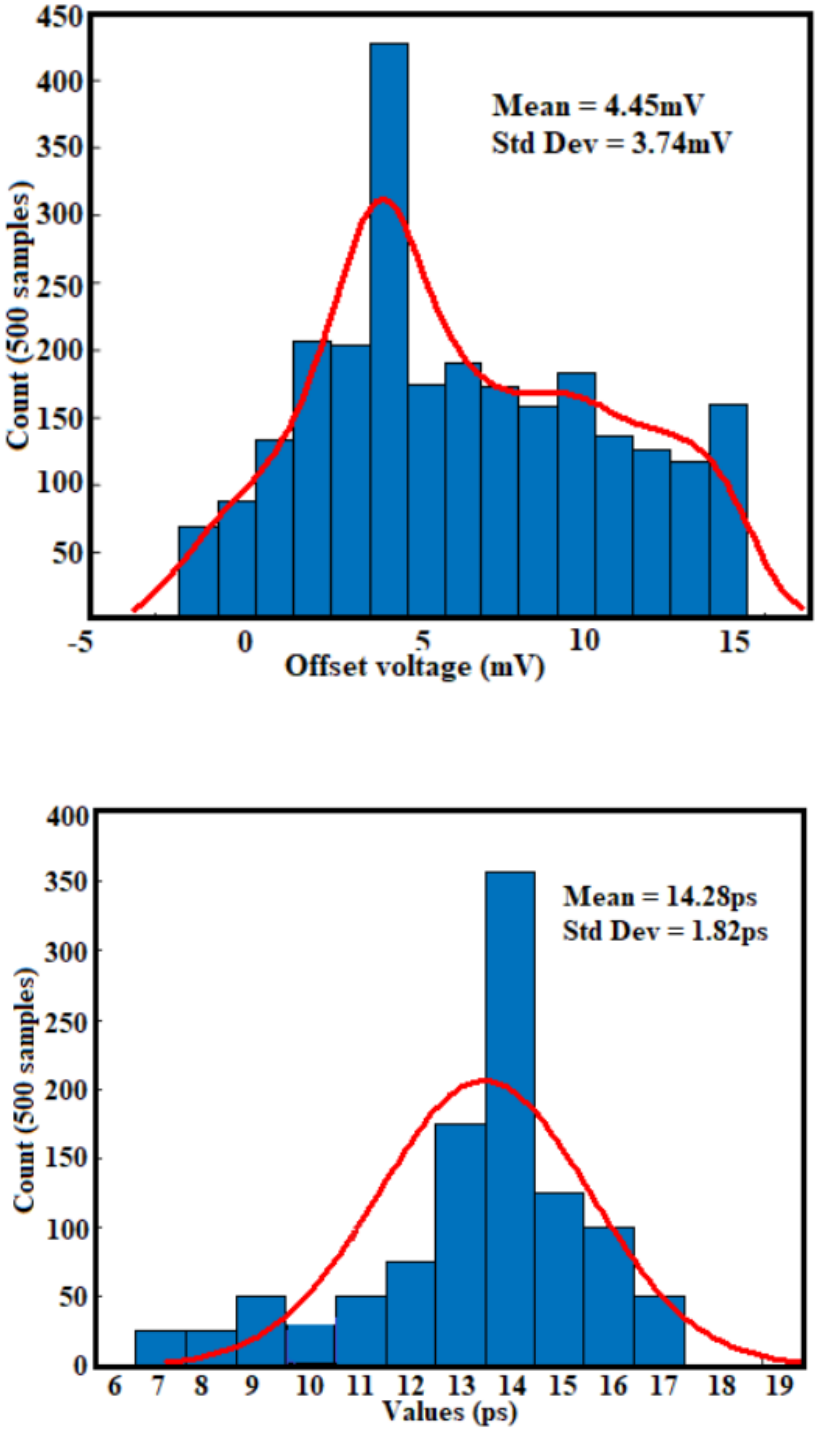


Figure.3.39. Monte Carlo results of both the offset voltage (a) and time delay of the proposed dynamic latch comparator (b) for 500 runs (VDD = 1 V, Vcm= 0.5 V, ΔVin = 0.5 V, Clk= 20 GHz, Cout= 3.8 fF)

3.5.3. Silicon implementation of the readout ASIC

The amplification circuit die area is only (256.2x80) µm^2 as shown in Fig.3.41. Parasitic extraction was used to extract the netlist with parasitic. The voltage supply is 3.3 V; the maximum power consumption achieved through post-layout simulations is about 8.72 µW for the whole circuit, which is 1.83% higher than that provided by the spice simulations. This little increase in power dissipation is mostly due to the parasitic and mismatch while laying out the design [132, 133 and 134]. In this research, the gain-bandwidth product of the circuit was stabilized by means of a high-frequency feedback loop, which operates according to the voltage-controlled NMOS resistor (R_F and Rp) technique [67, 115].

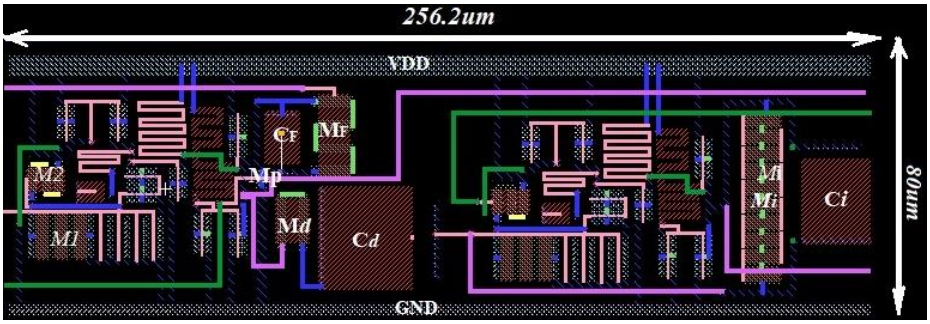


Figure.3.40. Core layout of the proposed readout FEE

The innovation of the proposed FEE results in the implementation of the external bandwidth compensation based adjusted gain stage, which allows achieving high gain with less among of current, preventing, therefore, the pulse height degradation along with bandwidth limitation and power dissipation. Further, the combination of the Miller compensation with the Feedback lead network is used to raise the best PM and guarantee decent stability of the gain-bandwidth product with good linearity for high-energy resolution applications.

The core circuit layout of the discrimination module is presented in Figure.3.42 where the chip occupies a small die area of 183.3 μm^2. The mismatch and parasitic capacitance were reduced during the design process, using a symmetrical and parallel placement of all the transistors of the circuits.

The full ASIC module was implemented and simulated to validate the design. For the first run, 33 fC input charge with 2.5 MHz flux rate are injected at the CSA input to produce a maximum shaping voltage of 1V from the base line. The available chip area was 1.8 mm^2, for a total of 40 input-output pads. The one channel ASIC consisted of CSA + PS and a dynamic latch comparator build of a preamplifier module, a latch stage and an output buffer circuit.

Two voltage power supply are (VDD1=1 V and VDD2 =3.3 V) provided, due to using 0.35 µm and 65 nm CMOS technology process for theses circuits. The different parts of the circuit shared the ground pad.

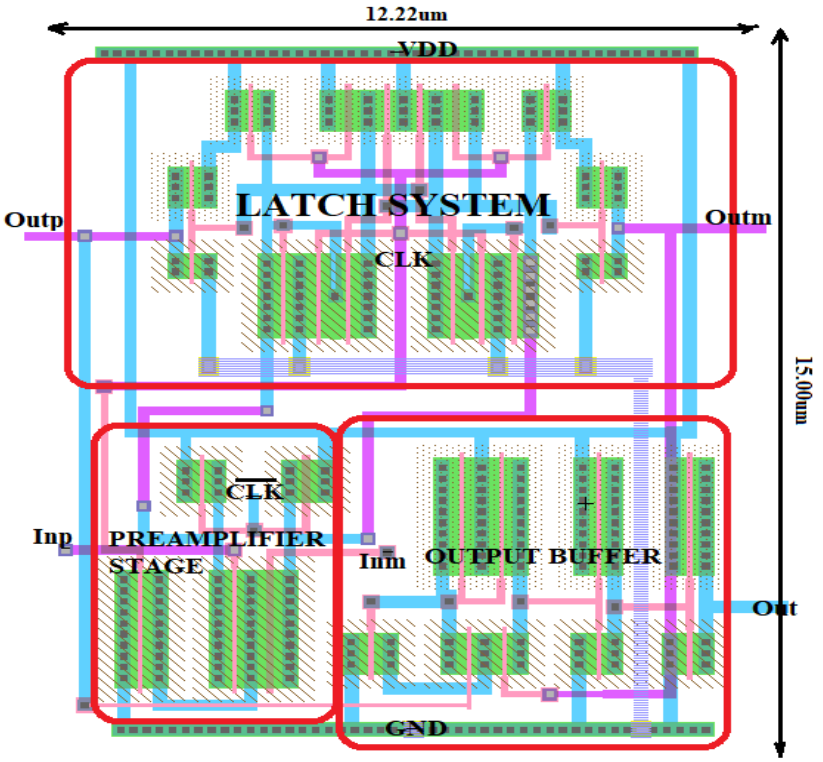


Figure.3.41. Layout diagram of proposed Dynamic Latch comparator using TSMC 65 nm CMOS technology.

Table 3.1.Extracted design parameters of the proposed CSA + PS modules

Transistor W/L(µm/ µm)	gmk value (µS)	Capacitance / λ
M1 - 62.5/10.5	gm1 - 61.4	C_L = 1 pF
M2 - 0.84/0.35	gm2 - 12.28	C_m = 50 fF
M3 - 18/0.35	gm3 - 50	C_F= 100 fF
M4,5,6 - 12/0.35	gm4,5,6 - 20	C_1= 0.74 fF
M7 - 9/0.35	gm7 - 200	C_2= 1.82 fF
M8,9 - 10/0.35	gm8,9 – 12	C_d= 534 fF
M_F – 3/36	gm_F – 13.13	C_i= 200 fF
M_P – 2.772/0.7	gm_F– 704.2	C_{L2}= 1 pF
M_d – 2/23.6	gm_d – 2.88	
M_i– 10/41	gm_i– 3.27	λ=0.0746
M_{1sh} – 3/20	gm_{ish}– 4.67	
M_{2sh} – 0.63/59.25	gm_{2sh} –0.467	
	$g_{03,08}$ – 0.1865	

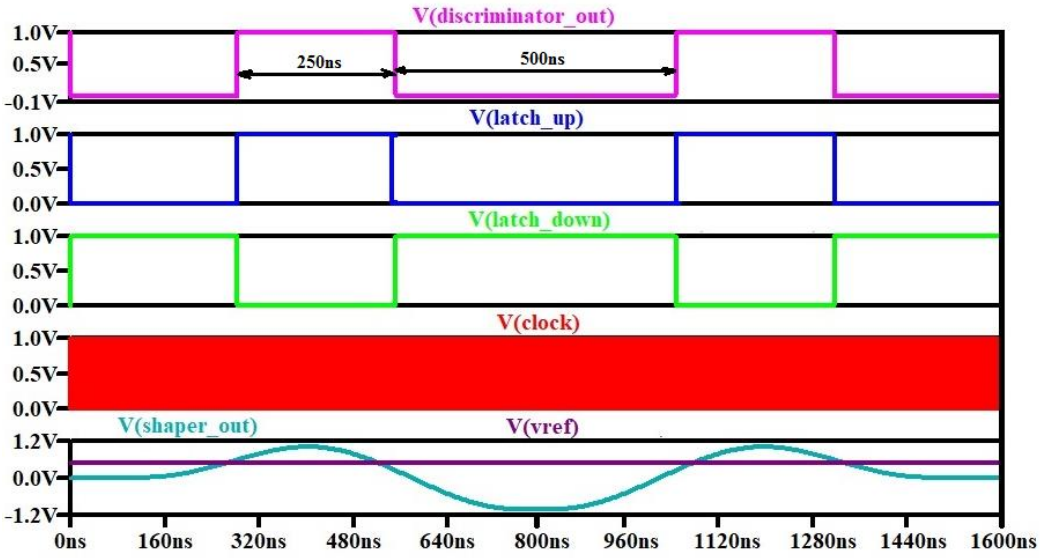


Figure.3.42: Simulation of the proposed ASIC for 33 fC input charge (with 5 GHz clock frequency).

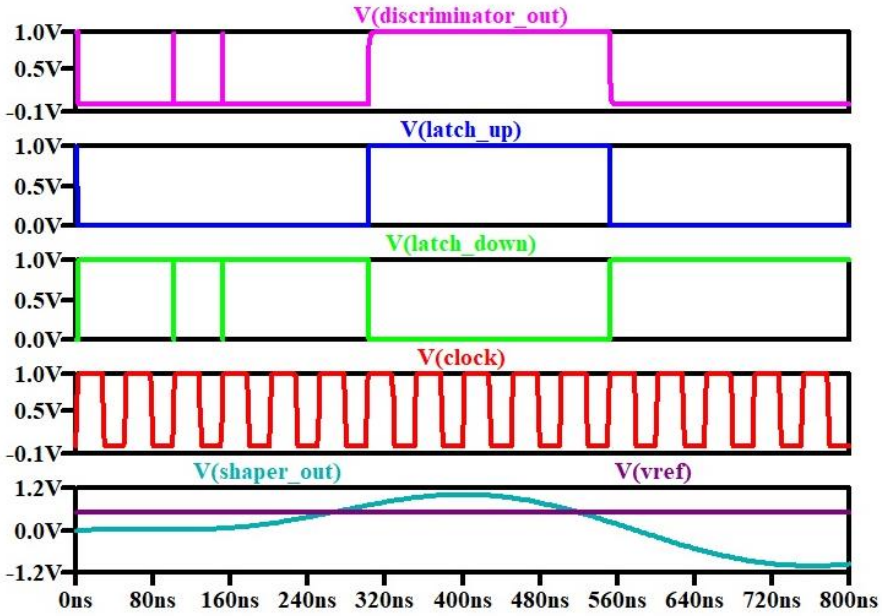


Figure.3.43: Simulation of the proposed ASIC for 33 fC input charge (with 10 MHz clock frequency).

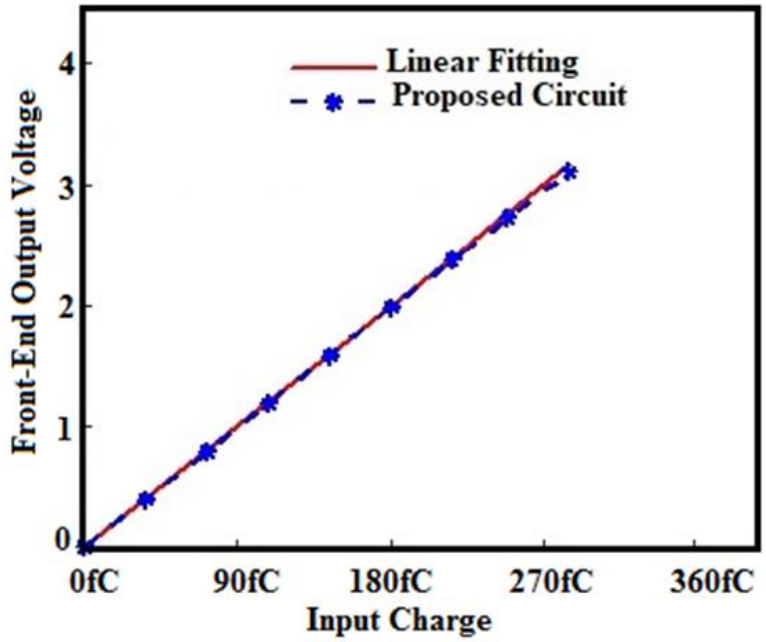


Figure.3.44: Linearity of the FE-ASIC from post layout simulation

3.5.4. PVT analysis of the ASIC module

Process variations outcomes worsen with reducing the channel length [118, 132, 133]. Mismatch being a function of threshold voltage (*VTH*) and supply voltage (*VDD*), low *VTH* (LVT) transistors have a reduced mismatch impact due to higher $\frac{V_{DD}}{V_{TH}}$ ratio than standard *VTH* (SVT) or high *VTH* (HVT) transistors the proportionate change in temperature from SVT to HVT is much larger as compared to that from LVT to SVT [43-45]. Thus, it is more advantageous to move from HVT transistors to SVT devices, but these results in high power dissipation. Large MOS devices increase the intrinsic parasitic capacitances, which lead to more thermal noise, but also reduce local head transfer and mismatch for LVT that can increase the power consumed by the design [134-137]. Taking into account the trade-off between transistor size and mismatch, we perform optimal transistor sizing/matching with a parallel arrangement of the devices to reduce the parasitic and mismatch effects. The maximum power consumption achieved by the amplification module (CSA + PS), was 8.72 µW as shown in Fig.3.36. The proportionate change in temperature from SVT to HVT is much larger as compared to that from LVT to SVT. Thus, it is more advantageous to move from HVT transistors to SVT devices, but this result in high power dissipation with the different corner process (FF and FS) for a temperature of 80˚C [127, 135]. Although the

increase in HVT can reduce percentage mismatch and power dissipation at temperature (-20˚C and 30˚C) for FF and FS corners. Large MOS devices increase the intrinsic parasitic which leads to more kickback noise and offset but also reduces local head transfer and mismatch for LVT [126, 135]. Taking into account trade-off between transistor size and mismatch, we perform optimal transistor sizing with parallel arrangement of the devices to reduce the parasitic and mismatch effects, cancelling therefore the short circuit power generated by those

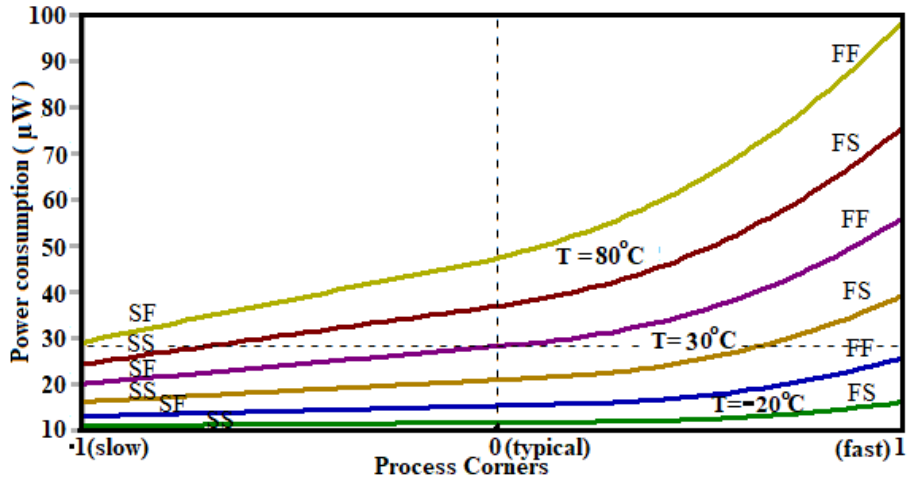


Fig.3.45. Corner analysis of the FE-ASIC showing power consumption versus process variations and Temperature

parasitic. Difference in NMOS and PMOS characteristics can create short-circuit power consumption [137]. Moreover, local mismatch effects on transistors can exacerbate the situation. The effect is relatively small compared to switching and leakage power. It can be shown on Fig.3.40 that SS and SF corners at different temperatures (-20˚C, 30˚C and 80˚C) were prone to ultra-low-power dissipation design, but would slow down the changing rate of the transistors. Such a condition would have a significant effect on input transistors (M16 and M17) of the preamplifier and the pull-up transistors (M9 and M10) of the latch, thus producing low-speed operations [135, 136,137].

3.6 Conclusion

This chapter has presented and discussed the results obtained in this thesis as the silicon detector readout ASICs are concerned. Based on theoretical analysis and transistor level design with spice simulations, photon detection front-end ASIC was proposed for high throughput and high-resolution purpose. A power-efficient ASIC based on low-noise CSA

and fast pulse shaper module has been designed in section 3.2. We found out that bandwidth limitation would affect the detection rate, lowering therefore the resolution of our system. Using an onchip solution would be good to target a specific bandwidth, but there might be not possible to control the gain bandwidth product (GBP). Therefore, an adjusting gain stage was implemented in the preamplifier stage in order to control the loop gain and compensated therefore the bandwidth limitation of the core amplifier. In section 3.3, we have paid attention on the noise behavior of the circuit. For the purpose, the ENC of the ciruit has been analysed and optimised for low-noise solution. The input transistor and the feedback resistors of the CSA module have therefore been designed to optimize the equivalent noise charge of the circuit. It has been derived and optimal peaking time of the post amplier stage. The feedback resistors were implemented using active MOS device based voltage-controlled resistor; this allows cancelling out the parallel noise contribution in the CSA, reducing energy loss in the shaper feedback capacitance and achieving an amplitude resolution of 1.87% FWHM therefore.

Section 3.4 was dedicted to the analysis and design of the discrimination system based latch type comparator. The major concerned in this stage were the optimization of the propagation delay and power consumption and the reduction of kickback noise. For these purposes, custom preamplifier based enhanced active NMOS load was designed to improve the regeneration speed and to reduce the power consumption of the dfesign. Short circuit current was reduced in the latch stage thanks to auxiliary transistors, which isolated the latch module to the ground state. The parasitic and mismatch were reduced adopting custom design and transistors matching/sizing during the design process. A compactarchitecture was therefore obtained and the regeneration process was speeded up. Offset and kickback noise were reducedand the time delay was improved.

The custom Front-End ASIC was validated in section 3.5. The CSA and shaping module achieved a charge to voltage conversion factor of 546.56 mV/MeV and 920.66 mV/MeV respectively, verified by the Monte-Carlo simulation results, and it is therefore compatible with the state-of-the-art. With a supply voltage of 3.3 V, the readout circuit consumes a maximum power of 8.72 µW. The post layout Monte-Carlo simulation outcomes reveal that the circuit achieves a maximum operating speed of 20 GS/s, with an average offset voltage of 4.45 mV and 3.74 mV standard deviation while propagating with 14.28 ps delay time with 1.82 ps standard deviation. Furthermore, theproposed comparator exhibited the lowest PDP of 0.968 fJ and dissipates only 67.8 μW of power.The percentage improvement in power

consumption for the designed comparator is 42% and 6% as compared to the conventional double-tailcomparator and comparator of ref [14] respectively. Moreover, the chiplayout of the proposed design occupies only 183.3 μm^2 *active* die area.The fast discriminator module was integrated to the chip for timing measurement. The ASIC was customized within a CMOS technology process and the achieved performances are much better comparing to recently published work. All the results obained find applications in many area such as High energy Physics, Medicine and Industry. For instance, the high speed dyanamic comparator can be also used in very high speed analog to digital converter (ADC) and our analog Front-End electronics can be used in multichannels radiation detection systems and multichannel readout recording of Electro-Encephalogram (EEG) and Electro-cardiogram (ECG) signals.

GENERAL CONCLUSION

2- Main results of this thesis.

This thesis has been devoted to the study and development of microelectronics and application specific integrated circuits (ASICs) chip for the readout of detectors. Motivated mainly by the need of solving the issue of photon arrival time and energy loss due to equivalent noise charge (ENC) and power dissipation, this work has aimed to set into analog integrated circuit design that found applications in particle physics, medicine and industry. We have presented in chapter one a review of literature on readout ASICs for semiconductor detectors. Some topologies involving analog front-end electronics and data acquisition board based filed programmable gate array (FPGA) have been presented. It has been discussed, some radiation effects on ASICs and provided therefore some design technique to cancel out these effects. Some applications of ASICs chip in high energy Physics, in medicine and industry have been presented.

Chapter 2 has emphasized with methodology of designing a one channel Front-End ASIC for single photon detection systems. First, the concept of integrating low-noise charge sensitive amplifier on-chip has been proved through a CSA circuit that exhibited internal feedback, which affects the bandwidth of the design. The need of compensating the bandwidth limitation and controlling an on-chip gain stage by an external device was therefore found suitable for achieving the lowest possible noise and high counting rate behavior of the circuit. We have therefore modelled a new architecture of the CSA circuit based small analysis. The adjusting gain stage was implemented and biased by typical current that produces the optimal dc-gain of the core amplifier. The input transistor has been optimized to exhibit low-noise and low power. Taking into account the post amplification stage, an optimal shaping time has been derived, and the lowest ENC of the circuit was achieved. Moreover, a Miller compensation with zero mulling resistor (MCNR) combined to an external feedback was used to cancel out the second pole in the transfer function of the CSA open-loop gain thus, stabilizing the gain-bandwidth product of the circuit. A custom feedback network basedvoltage-controlled NMOS resistor was also implemented to cancel out the parallel noise of the passive feedback resistor in the CSA module.

For an accurate timing measurement purpose, a fast discriminator based dynamic latch comparator was presented and discussed. The design techniques for achieving low-offset,

low-power and high speed have been clearly presented and discussed. For the purpose, the comparison process has been speed-up and the power dissipation reduced to a great extent using a custom differential pair based NMOS active load in the preamplifier stage. The decision making process has also been speed-up using auxiliaries transistors that isolates the cross-coupling inverter to ground, increasing therefore the effective transconductance of the cross-coupling mechanism. A particular attention has been paid for reducing mismatch and parasitic while laying out the circuit. Short circuit power dissipation has been therefore avoided, and the total time delay of the circuit has been reduced. The discriminator was therefore build.

In chapter 3, the results and discussion of the work have been reported. We have mainly focused on the implementation of the Front-End ASIC made of a CSA a PS module and a discriminator based dynamic latch comparator. The results have been structured into four parts. In the first part, the optimization of the charge extraction and shaping process leads to designing the lowest possible rise time of the CSA compared to the peaking time of the shaping amplifier; this would prevent ballistic deficit, which involves loss of resolution.The following results have been obtained:

- At a critical biasing current of 2.5 µA, the CSA achieved a sufficient open loop gain and bandwidth, which guaranteed 7.36 ns, charge collection time. For the purpose, a common-source (CS) input design has been adopted in the CSA module, to isolate the input capacitance, preventing it from affecting the bandwidth.
- The stability of the CSA was guaranteed with 82 degrees phase margin, thanks to a Miller compensation with zero mulling resistors (MCNR) combined to an external feedback that has been used to cancel out the second pole in the transfer function of the CSA open-loop gain thus, stabilizing the gain-bandwidth product of the circuit.
- The offset voltage at the CSA stage has been reduced thanks optimizing the biasing current of the internal gain stage. In fact, the transient simulation of the CSA output voltage versus the biasing current shows that dc-component of the CSA was sensitive to the biasing current. This was due to temperature and threshold voltage variations, involving drain induced barrier lowering effects (DIBL). To avoid this, the bulk-source voltage of all MOSFETs has been biased to exhibit no threshold variation. It has come therefore acritical current that optimize the offset voltage.

- It has been also observed the peak pile-up effect; which lowers the energy resolution of the design. That effect, which occurs at the CSA output, has been canceled out using a pole zero canceller circuit.
- Finally, taking into account previous considerations, in the pulse shape anenergy-efficiency of the FE-ASIC has been guaranteed by improving the charge conversion process in the shaper circuit and optimizing the power consumption to less than 10 µW.

In the second part of chapter 3, we have dealt with the noise behavior of the front-end and its optimization technique. Since the parameter that embodies the noise aspect in nuclear instrument is the equivalent noise charge (ENC); it has been optimized with regards to the detector capacitor first, secondly the ENC has been optimized by designing the input transistors of the CSA and PS circuits respectively. Finally, the ENC has been optimized with regards to the shaping time which allows guarantee the high counting rate behavior of the proposed circuit. The following results have been obtained.

- The variation of the ENC as a function of I_D and W was computed and presented.

While increasing the current in the input transistor, its thermal noise decreases but the bandwidth over which the thermal noise is integrated increases by the same amount; those effects cancelling each other out. By reducing, the bias current of the input transistor provided a good reduction of thermal noise.

- The variations of the ENC versus the peaking time shwo that at some peaking time the noise is minimum. That optimal peaking time garanteed the higherst signal-to-noise ratio achieved by our design. At short peaking times, the noise increases rapidly with capacitance and increases as the peaking time is reduced. This noise is only weakly dependent on temperature. At long peaking times, the noise increases with peaking times and with leakage current. So, the total ENC of the front-end has been optimized with regards to peaking time.

- The intrinsec ENC behavior of the circuit has been analysed agains power dissipation. It has come that the ENC was reduced when the power dissipation increases. The ENC achieved a minimal value of 37.8632 e^-rms when the power dissipation was larger than 8.56 µW. This means that the specification of the power dissipation satisfies the design requirements.

- The effects of the CSA gain bandwidth on the ENC have been analyzed with several input transistor widths. It is readily recognized that lower transistor width leads to

higher thermal noise for GBW from 1 to 20 dB. This is because for lower GBW, the collection process is slowed down; due to the highest rise time, the thermal noise accumulated in the device increases accordingly. This results in the attenuation of the output swing and therefore a poor energy resolution. This issue has been solved by designing the critical transistor width for which the variation of the thermal noise is not sensitive to the CSA gain bandwidth.

The third part of chapter 3 is devoted to the pulse shape discrimination based fast dynamic latch comparator. The studies carried on in this part will help to solve the problem of quantization errors found in fast timing measurement systems and fast counting rate events. Indeed we have examined the problem of comparison speed and power consumption in the dynamic latch comparator. Three major parameters have been identified and a compact architecture of the comparator was proposed for handling fast speed operations the achievements of this designed module can be summarized as:

- The comparison speed has been achieved using custom differential pair based NMOS active load in the preamplifier stage. In fact, the inconvenient of an NMOS to drive V_{DD} - V_{THN} when its gate and drain are clocked to V_{DD}; comparing to the PMOS counterpart in which nodes drives V_{DD} in the same conditions, has been used as an advantage in our design.

- The decision making process of the comparator has been speed using a custom latch circuit. In fact, the effective transconductance of the cross-coupling transistors consisting the latch has been improved through auxiliary devices. The analysis of the time delay versus the width of the auxiliary switches shown that delay decrease exponentially when width increases, but for width larger than 3 µm the delay achieved a constant value. So, increasing the width would not help to reduce significantly the delay.

- We achieved low-offset thanks to using auxiliary switches. In fact, at the beginning of the comparison phase, these auxiliary transistors are turned on and help the circuit to start the decision-making and then the regeneration process. The devices are biased to operate in triode region and help in keeping the drain of the input transistors to sense a less voltage variation, which leads to less kickback noise.

- We have demonstrated the dependency of the proposed comparator delay on various differential input voltage levels at different supply voltages. The delay decreases exponentially when the differential input voltage is increasing. It has come that, at a particular differential input, the higher the supply voltage (V_{DD}), the higher the comparator delay will be. We targeted therefore for 1 V supply voltage in the discrimination module.

- Finally, the effects of the input common-mode voltage (*Vcm*) on the delay of the comparator has been explored for 500 mV differential input under different supply voltages, and the results shown that,for a fixed value of V_{DD}, the delay decreases while the input common-mode voltage (*Vcm*) increases.

In the last part of chapter 3, particular attention has been paid to design validation and silicon implementation of the proposed Front-End ASIC. The challenge was the implementationof low-noise, low-power and high energy resolution integrated circuit on a very few chip of silicon. Taking into account the previous achievements, the following results have been obtained therefore.

- The pileup and offset compensation effects help in increasing the conversion gain. The post layout simulation of the ASIC agains radiation has been performed and the exhibited high conversion factor and high-energy resolution under radiation hardness.

- The post layout Monte-Carlo simulation outcomes shown that the systems achieved lower ENC along with very less power consumption. Comparing to that obtained in spice simulation, the little variation of power consumption and ENC provided by the post layout analysis proves the presence of parasitic while layout the circuit.

- Finally, corner analysis has been performed through process voltage and temperature variations. The circuit has been simulated under different corner process with several temperature conditions. Since large MOS devices increase the intrinsic parasitic capacitances, which lead to more thermal noise, low *VTH* (LVT) transistors have been chosen to reduce mismatch effects. The overall power dissipation of the custom ASIC along with its total thermal noise was stabilized and the circuit exhibited low-power and low-noise behavior.

From the results of this thesis, we can claim that an on-chip gain stage in the CSA controlled by an external device is a good solution for extending the bandwidth Front-End and achieving therefore fast charge collection process along with assuring the higher energy resolution and higher counting rate behaviour of the design. Finally, this study contributes to solve the problem of time delay and kickback noise in fast discrimination systems based latch type comparator.

3- Perspectives of the work

The front-end electronics (FEE) of the Compact Muon Solenoid (CMS) is still needed very low power consumption and multichannel readout ASICs to match the low power requirement of its short strip ASIC (SSA) and to handle the large number of pileup events which occur in the High-Luminosity Large Hadron Collider (LHC) for more than 10 MHz particle flux rate. This will necessitate a full custom multichannel ASIC made of 128-channels anlog front-end multiplexed into one analog to digital converter (ADC). Most of the nuclear spectroscopy applications require multiple channels performing in parallel. Nowadays, field programmable gate arrays are the devices that offer parallel and reconfigurable resources for complex control algorithms. With the new hybrid system on chip (SoC) devices, which consists of field programmable gate array (FPGA) and microprocessor tightly coupled in the same silicon not only provide high density logic- arithmetic resources but also other services like communication with PCs with high data throughput. Therefore, the output of the ADC should process by a data acquisition system based FPGA.

- The first challenge would be the integration of 128-channels of detection on a single chip, while preserving energy efficiency and low-noise behaviour of the circuit.
- The second challenge would be the implementation of a fast and high resolution ADC to digitize all the 128-channels analog output.
- Implementation of the data acquisition system based on programmable SoC devices.

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LIST OF PUBLICATIONS

1. Journal papers.

1- **Jérôme, F.K**.; Evariste, W.T.; Bernard, E.Z.; Crespo, M.L.; Cicuttin, A.; Reaz, M.B.I.; Bhuiyan, M.A.S. "An 8.72 µW Low-Noise and Wide Bandwidth FEE Design for High-Throughput Pixel-Strip (PS) Sensors", ***Sensors*** **2021, *21*, 1760** (**IF=3.576**).

2- **Folla J.K**, Maria L. Crespo, Evariste T. Wembe, Mohammad A. S. Bhuiyan, Andres Cicuttin, Bernard Z. Essimbi and Mamun B. I. Reaz. "A low-offset low-power and high-speed dynamic latch comparator with a preamplifier-enhanced stage." **IET Circuits DevicesSyst. 2021; 15:65–77 (IF=1.676).**

3- **F. K. Jérôme**, W. T. Evariste, E. Z. Bernard, M. L. Crespo, A. Cicuttin, M. B. Ibne Reaz, M. A. Sobhan Bhuiyan and M. E. Hoque Chowdhury. "Low-noise stable Charge Sensitive Amplifier for Silicon Detectors Applications" **Informacije Midem, 50, (1), 3 – 13, (2020) (IF=0.446).**

2. Conference paper

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Article

An 8.72 µW Low-Noise and Wide Bandwidth FEE Design for High-Throughput Pixel-Strip (PS) Sensors

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Abstract: The front-end electronics (FEE) of the Compact Muon Solenoid (CMS) is needed very low power consumption and higher readout bandwidth to match the low power requirement of its Short Strip application-specific integrated circuits (ASIC) (SSA) and to handle a large number of pileup events in the High-Luminosity Large Hadron Collider (LHC). A low-noise, wide bandwidth, and ultra-low power FEE for the pixel-strip sensor of the CMS has been designed and simulated in a 0.35 µm Complementary Metal Oxide Semiconductor (CMOS) process. The design comprises a Charge Sensitive Amplifier (CSA) and a fast Capacitor-Resistor-Resistor-Capacitor (CR-RC) pulse shaper (PS). A compact structure of the CSA circuit has been analyzed and designed for high throughput purposes. Analytical calculations were performed to achieve at least 998 MHz gain bandwidth, and then overcome pileup issue in the High-Luminosity LHC. The spice simulations prove that the circuit can achieve 88 dB dc-gain while exhibiting up to 1 GHz gain-bandwidth product (GBP). The stability of the design was guaranteed with an 82-degree phase margin while 214 ns optimal shaping time was extracted for low-power purposes. The robustness of the design against radiations was performed and the amplitude resolution of the proposed front-end was controlled at 1.87% FWHM (full width half maximum). The circuit has been designed to handle up to 280 fC input charge pulses with 2 pF maximum sensor capacitance. In good agreement with the analytical calculations, simulations outcomes were validated by post-layout simulations results, which provided a baseline gain of 546.56 mV/MeV and 920.66 mV/MeV, respectively, for the CSA and the shaping module while the ENC (Equivalent Noise Charge) of the device was controlled at 37.6 e^- at 0 pF with a noise slope of 16.32 e^-/pF. Moreover, the proposed circuit dissipates very low power which is only 8.72 µW from a 3.3 V supply and the compact layout occupied just 0.0205 mm^2 die area.

Keywords: ASIC; CMOS technology; compact muon solenoid; integrated front-end electronics; low-noise; low-power; radiation sensor

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1. Introduction

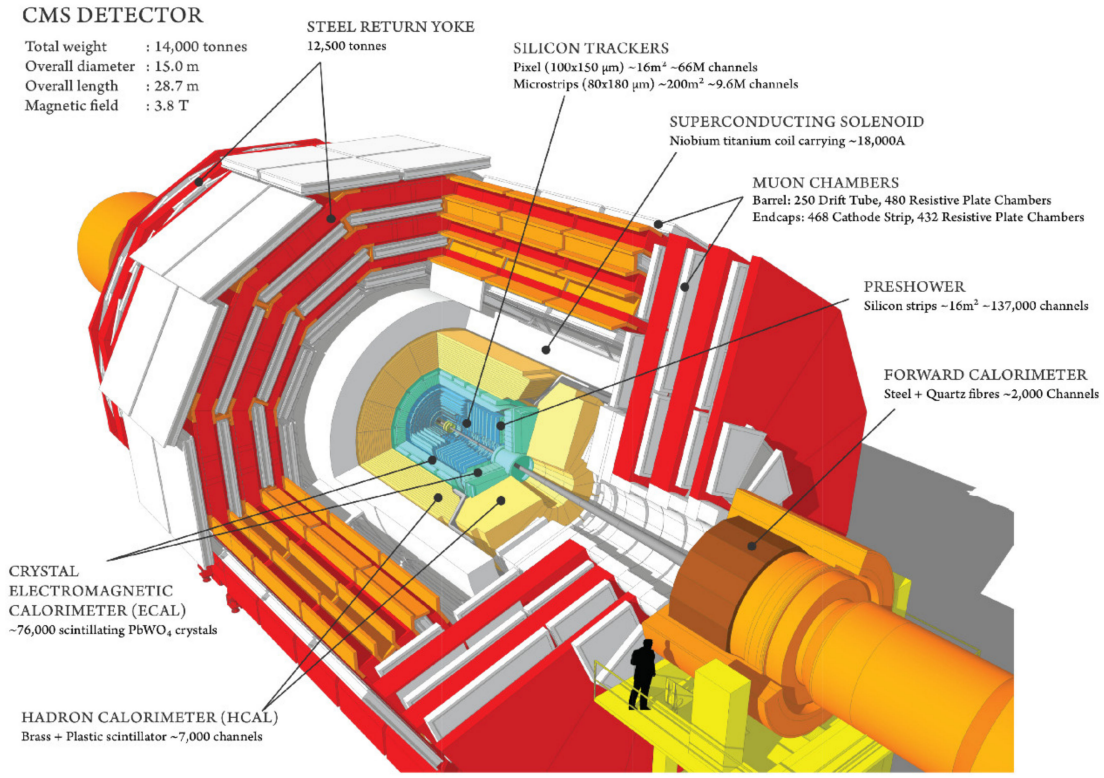
The front-end readout system for modern High Energy Physics Experiments (HEPEs) is a mixed-signal circuit, which performs precise measurement of particle trajectories. It amplifies the output signal of the photon sensor. A data acquisition (DAQ) based Field Programmable Gate Array (FPGA)-based board then extracts all necessary data about the

photons from the output signals of the readout electronics and utilizes that information to figure out a coincidence pair of photons to create a line of response (LOR) [1–4]. For instance, the Compact Muon Solenoid (CMS) illustrated in Figure 1a [5], is predicted to receive a substantial upgrade of the outer tracker sensor and its front-end readout electronics, needing higher granularity and readout bandwidth to absorb a big amount of pileup events in the High-Luminosity Large Hadron Collider (LHC) [2,5]. Therefore, the whole tracking system will be substituted with highly radiation-tolerant sensors which will be capable of handling higher readout bandwidths and particle flux rates [2,5].

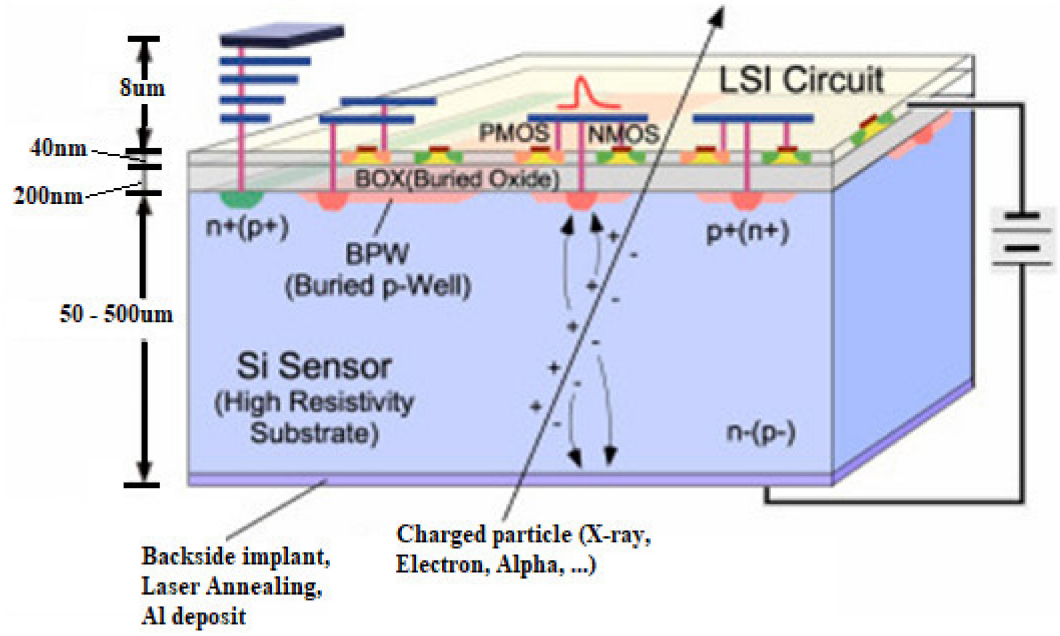
To recognize particles having higher transverse momentum (>2 GeV/c) and to distinguish the front-end output with a given L1 trigger level, a double layer sensor module, which combines a pixel sensor with a strip one, was adopted. Consequently, two different readout application-specific integrated circuits (ASICs) were developed, namely the Short Strip ASIC (SSA) for the strip sensor and the Macro Pixel ASIC (MPA) for the pixelated sensor [2,5,6]. The operating principle of a pixel-strip sensor is illustrated in Figure 1b [7]. As ionization is produced on each strip, and the readout circuit should process the ionized particles; therefore, in order to handle higher particles flux, SSA is needed to be implemented within a Complementary Metal Oxide Semiconductor (CMOS) process and integrated into the sensor's chip [2,5]; this will avoid loss of transmission between the high-speed interconnects and the readout ASIC chip [8–11].

Recent research on pixel-strip sensors reveals that those devices can transform gamma rays to charges operating at normal temperature, which exhibits a better potentiality for the detection of X-rays and γ-rays for possible nuclear instrumentation applications [6]. A typical thickness for Si-sensor is about 300 μm; the limiting irradiation energy, which would penetrate protons through the sensor, is about 6.2 MeV [5,7]. With moderate cooling by means of small Peltier cells, silicon drift detectors and Si-PIN sensors show particularly excellent spectroscopic performances and good detection efficiency below 15 keV [5,11,12]. In contrast to the spectroscopy amplifier, the major concern for a fast amplifier is the preservation of the charge collection process while keeping a wide bandwidth, which in turn optimizes the signal rise time [4,5,9,12]. The improvement of energy resolution leads to optimization of the charge collection process by designing the lowest possible rise time of the charge sensitive amplifier (CSA) compared to the peaking time of the shaping amplifier; this would prevent ballistic deficit, which involves loss of resolution. Therefore, the energy sensitivity of the readout module should be high enough to minimize the energy loss and guarantee a high rate collection process, which is characterized by its rise time (tr) and can be performed in less than 10 ns to guarantee high counting rate operations [4]. Moreover, for multi-channel readout electronics, the spatial resolution should be more than 2 μm [4,5,12].

A big amount of channels can be made feasible using large-scale integration to include the associated electronics on the same chip of the sensor. Silicon sensors offer a typical signal in the range of tens of thousands of electrons within a collection time of few nanoseconds that should be processed by a readout integrated circuit (ROIC). Signal processing starts with the integration of the input signal, a very small and fast current pulse, into a voltage step performed by CSA [8–10]. The CSA output swing is proportional to the total integrated charge, which is in time proportional to the energy released by the incident particles in the sensor. This energy must be measured with the highest accuracy and precision [2,3]. The input node voltage of the CSA increases (tends to increase) and the voltages with the opposite polarity are generated at the output terminal simultaneously. Hence, the output potential through the feedback loop forces the input potential of the CSA to become zero because of high open-loop gain as shown in Figure 2.



(**a**)



(**b**)

Figure 1. (**a**) The building blocks of the Compact Muon Solenoid (CMS) [5]. (**b**) Principle of operation of a silicon pixel-strip sensor [7].

The input current pulse is integrated into the feedback capacitor and the corresponding output is a step voltage pulse [6,7,10,13,14]. This voltage is filtered and digitized by an Analog to Digital Converter (ADC) as shown in Figure 2. The resulting data are then coded into an appropriate format so that pixel address, time, amplitude or transverse momentum [5,12] can be extracted through an FPGA module for further processing [11,15].

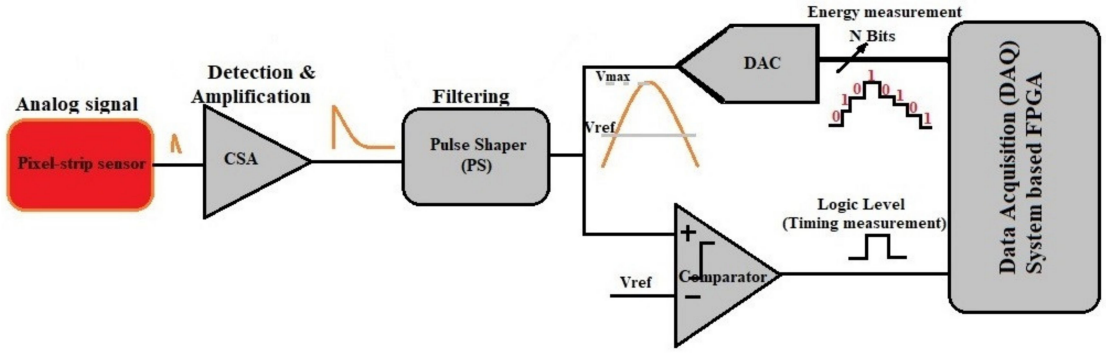


Figure 2. Pixel-strip sensor readout architecture for digital processing, the Charge Sensitive Amplifier (CSA) is used for extracting the charge at each strip and convert it into voltage.

It is well known that the input signals intercepted by CSA are generally very low in the range of few fC ($\sim 1fC$) charges. For a given source, the generated preamplifier noise and the input impedance of the amplifier influence the front-end noise performance. The impact of radiations on the devices exacerbates the situation [9,11,12,16,17]. Therefore, the front-end input stage must ensure that optimum noise matching is achieved for the source impedance [11,12,17]. The design parameter of the input stage of CSA directly influences the noise matching. So, the equivalent input noise should be kept as minimum as possible for a given sensor capacitance. The main problem in the design of nuclear spectroscopy very large scale integration (VLSI) readout front end is the implementation of low-noise and low-power CSA. CMOS exhibits several advantages over other concurrent technologies (such as Bipolar, BiCMOS, etc.) and therefore, usually preferred to design application-specific integrated circuits (ASICs) [6,14,18,19]. A widely accepted front-end electronics (FEE) design approach is the use of an operational amplifier (Op-amp), with the R-C feedback network. However, this needs large sensor capacitance (about 15 pF), which compromises the stability of the design [6,14]. The stability, conditions are indicated by the phase margin (PM) and the gain-bandwidth product (GBP) within the Bode plot for the design of single-stage and two-stage amplifiers. However, the stability of multistage amplifiers requires advanced computations than single-or two-stage amplifiers; resulting from the existence of complex poles in high-order switch capabilities [6,20,21]. In addition, the desired performance requirements (GBP, PM) rely on the frequency compensation method and the value of the load capacitance C_{L1}. For a complete validation of the front-end electronics with CMOS technology, the overall system specifications are needed [20–22]. In ref. [22], H. Wang et al., proposed readout electronics with CSA-based Polyvinylidene Fluoride (PVDF) transducers. The circuit works for low power dissipation and low frequency, but it was prone to low conversion gain, high feedback capacitance that occupies more die area. Moreover, due to several biasing points, that circuit was prone to more threshold variation and exhibited a higher dc-component, which worsen the output swing of the design [23,24]. In ref. [23], Haryong Song et al. proposed the Ripple Rejection Loop (RRL) techniques for mismatch reduction and offset cancellation in the input transistor stage. The technique works for low-frequency applications. However, the RRL circuit for X-rays and gamma rays spectroscopy could be implemented at the expense of some flicker noise and radiation damage [24,25], in high frequency. Moreover, due to power consumption requirements and hit transfer, the on-chip implementation of the RRL circuit is huge and is therefore not encouraged for spectroscopic purposes.

In recent years, radiation effects have become an important issue in semiconductor readout systems. Radiation hardened devices are constrained by the technology [7,9,26]. Scaling down technology leads to lowering the gate-oxide thickness, involving variations in threshold voltage (Vth) and inducing radiation damage. The reduction of threshold voltage shift (Vth variations) leads to minimizing the gate-oxide thickness (t_{ox}) [9,26], then increasing the probability of quantum tunneling of electrons, which enables, therefore, most

of the trapped holes caused by induced radiation to be recombined with electrons [26]. The low-threshold voltage (LVT) operation of subthreshold circuits applies lower electric fields across the gate-oxide [27]. This will reduce the rate of electron-hole separation and increase the probability of recombination. Therefore, this induces a lower trapped charge in the oxides and hence lower will be the radiation-induced threshold voltage shift and leakage current. Reducing variation of Vth helps the MOSFET device become more radiation-tolerant (more robust to radiation) [7–10,26]. A. Baschirotto et al. [20], designed a front-end using a single-ended amplifier as CSA. The circuit works at high frequency and very low voltage; however, the disadvantages of that circuit are high power consumption and high equivalent noise charge (ENC) which worsen the radiation-hardened behavior of the circuit [9,19,25,28,29]; furthermore, the circuit was prone to more parallel noise generated by the passive feedback resistor. The main problem in designing nuclear spectroscopy very large scale integration (VLSI) readout front ends is the execution of low-noise and low-power CSA, which guarantees high particles flux with the lowest pulse pile-up. Therefore, a good choice in the pulse shaping parameters is crucial for achieving good energy resolution and minimum pulse pile-up for high counting rates [11,30,31]. For high throughput experiments, short shaping time (τ_s) reduces the pile-up effects and for an optimal design solution, the minimum τ_s limits the charge collection process and increases the energy resolution accordingly [4,12,25–32]. Therefore, it is necessary to propose an optimal front-end circuit to avoid unnecessary power dissipation and heat in closely packed pixel arrays first avoid. Secondly, the ENC should be optimized concerning sensor capacitance along with the shaping time and the input transistor width, for performing AC and transient analysis and finally, the core amplifier should guarantee a high loop gain, wide bandwidth, high stability and very low-power consumption [6].

This work describes the design and simulation of an ultra-low-power, low-noise and wide bandwidth FEE for high throughput pixel-strip sensors. The circuit consists of a three-stage single-ended CSA followed by a one-order Capacitor-Resistor-Resistor-Capacitor (CR-RC) pulse shaper (PS). The originality of this research results in the following statement; a modified CSA topology was designed for ultra-low-power and high counting rate solution. To compensate for the bandwidth limitation and achieve good stability along with preserving the pulse height degradation, an adjustable gain stage over a wide input dynamic was implemented and controlled by an external device. For this purpose, a common-source (CS) input design is adopted to segregate the input capacitance in order to avoid any bandwidth adjustment. Further, a Miller compensation with zero nulling resistors (MCNR) combined with external feedback was used to cancel out the second pole in the transfer function of the CSA open-loop gain thus, stabilizing the gain-bandwidth product of the circuit. A custom feedback network-based voltage-controlled N-type Metal Oxide Semiconductor (NMOS) resistor was also implemented to cancel out the parallel noise of the passive feedback resistor in the CSA module. A simple and optimal pulse sharper circuit was designed for achieving the highest possible signal-to-noise ratio (SNR) to allow a scale adjustment in energy resolution [11,12,32–38]. Further, rigorous transistor sizing/matching was performed to reduce the mismatch and achieve an ultra-low-power behavior of the circuit while assuring the radiation hardness behavior of the design [37–42]. The rest of the paper is organized as follows: Section 2 provides the design philosophy and materials. Analysis related to the CSA and shaper architectures are discussed, the design parameters are derived and implemented; therefore, the proposed front-end is validated and simulated. In Section 3, the achieved results are discussed. The paper is concluded in Section 4.

2. Design Philosophy and Materials

As illustrated in Figure 2 the global diagram of the front-end electronics is presented. The circuit consists of a CSA as a first stage followed by a differentiator and a one stage integrator as the shaping stage, which further amplifies the CSA output signal and optimizes the signal to noise ratio (SNR). This constitutes one channel of detection. The sensor,

with a capacitance C_{det}, produces current pulses that are integrated on the CSA feedback capacitor C_F [6,25,26,33]. To reduce the pile-up, it is necessary to use a short peaking time. The tradeoff of bandwidth, pulse rise time, peaking time and counting rate is necessary for the selection of the topology of the CSA core Op-Amp [4,25].

Several high gains with wide bandwidth CMOS Op-Amps have been developed and conveyed recently. Those topologies usually employ three to five gain-boosting stages to ensure high gain and mostly necessitate a number of compensation capacitors [34]. It is clear from the literature that the enhancement of the amplifier gain is achieved because of adopting positive feedback, which in turn produces a compensating negative conductance [29,35]. However, in most of those structures, the positive feedback generates a negative resistance at the output node, which produces high DC gain by compensating some of the positive resistance at the output [30,31].

The self-cascode structure also known as composite cascode structure is sometimes used to control the gain of CMOS Op-Amp, since they are built by cascading common source with a common gate; the structure offers a larger effective channel length and a larger effective output resistance [32]. However, at higher frequencies, the output capacitor starts shorting out, providing a low impedance path to the small-signal current and thus there is a decrease in gain. Combining this with the high DC-gain produced by the positive feedback structure will exacerbate the situation and introduce a poor gain measurement at high frequencies [34].

2.1. Design of the CSA Core Amplifier Circuit

For high-speed applications, the GBW of the CSA must be made maximized [4,25]. To overcome the bandwidth limitation and improve the amplitude resolution for excellent particle identification ability, the GBW of the preamplifier is extended to achieve an output rise time of about a few ns as a response to impulsive charge [4]. This requires therefore high input transistor transconductance (gm) [6,28,34]. However, increasing the gate transconductance of the input transistor for a given drain current deals with increasing the device channel width and total gate capacitance, which worsens the electric noise. Therefore, optimizing the sizes of the MOSFETs would lead to a more radiation tolerant circuit [9,10]. Most of the shortcomings of the previous section can be eliminated by custom transistor sizing during the design process [28,30–32] along with implementing an internal compensation. In the former case, the compensation network is fabricated on the chip, and usually, no external access to the compensation network is provided [37]. A custom compensation technique in which the CSA GBW is adjusted by an external device is proposed. The proposed CSA has been designed in 0.35 μm technology from the TSMC process. The input transistor aspect ratio Width/Length (W/L) was suitably designed for low-noise and high gain purposes [11,12]. Moreover, an on-chip gain adjustable stage was implemented to extend the bandwidth of the core amplifier. An external resistor through a bias current controls this adjustable gain stage. A custom feedback network was adapted to perform the initial conversion of small current pulses into voltage step pulses. Table 1 presents the design specifications of a CSA circuit for typical Silicon-PIN sensor applications. To increase the gain of the CSA, we studied a three-stage configuration for the design. The single-ended configuration of the circuit exhibited in Figure 3, is more appropriate than the differential one for the reduction of power consumption. The choice of the N-channel input transistor relies on the lower thermal noise compared to the P-type at high frequency [9,18], since the 1/f noise is negligible in the frequency region above 10 kHz [6,38,39]. In addition, N-channel MOS, gives a lower series white noise with respect to the P-channel counterpart, because of its higher transconductance [6,27,38] at the same drain current compared to the PMOS device. The current source at M_1's drain is provided by M_2, which is a P-channel MOSFET with smaller transconductance.

Table 1. Required CSA specifications for silicon sensors for two vendors [6].

Vendor Parameters	Hamamatsu (H4083)	AMPTEK (A250)
Power consumption	50 mW@12 V	14 m W@6 V
Count rate	2.6 MHz	2.5 MHz
Sensor capacitance	0–25 pF	0–250 pF
ENC (Cin = 5 pF)	240 e^-	6 e^-
Noise slope	4 e^-/pF	11.5 e^-/pF
Sensitivity	22 mV/MeV (Si)	176 mV/MeV (Si)
DC gain	94 dB	76 dB

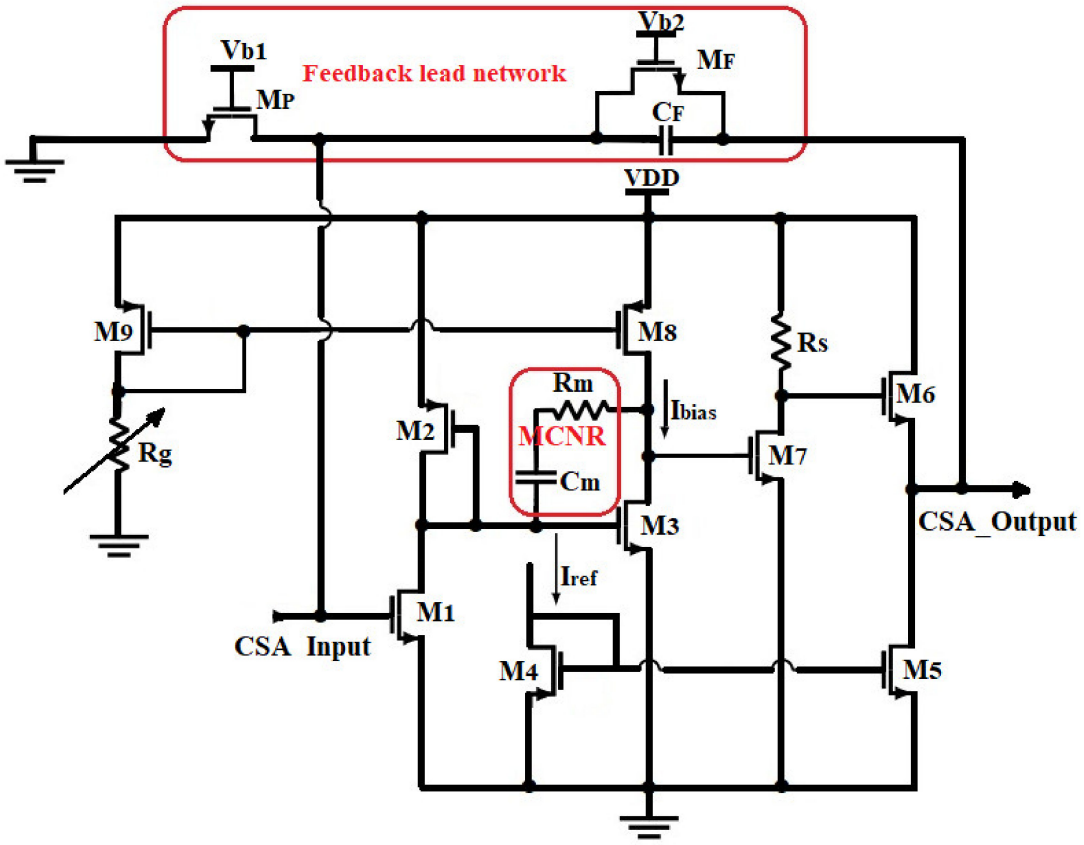


Figure 3. Schematic of the structure of the proposed CSA.

The second stage is a common-source based current load, so that the drain current of M_8 (I_{bias}), is used to adjust the dc-gain of the amplifier. It utilizes a Miller Compensation combined with a custom feedback module for achieving good stability of the design. The stability of the feedback capacitor (C_F) and the preamplifier open-loop gain determine the reliability of the preamplifier sensitivity. The open-loop gain is usually quite large, and hence the effect because of the small changes in the C_F can be ignored [39,40].

Therefore, the bias current is kept at a specific low value (2.5 µA) to keep a very low transconductance of M_3 thus, exhibiting very high loop gain. Capacitor C_m provides gain and the dominant pole in that stage; so, a resistance R_m is used to suppress direct transmission through C_m at high frequencies [18]. Such a stage in the CSA incorporates a higher output resistance. All the transistors should be kept in their saturation state, i.e., $V_{GS} > V_{TH}$ and $V_{DS} > V_{GS}$-V_{TH} [6,39] to provide the maximum output swing for this stage. Here V_{TH} values for NMOS and PMOS are 0.6 V and −0.85 V, respectively.

The third stage consists of an N-channel MOSFET M_7, which aims to give a negative gain of the entire circuit so that one can apply the negative feedback. It is biased by a low current through R_S. The value of Rs is set to 3 kΩ so that M_7 should operate in the

saturation region. The output stage is source follower based, designed to exhibit unity voltage gain. Current flow from M_4's drain kept M_5 biased in saturation. The feedback loop is built of an on-chip feedback capacitor C_F of 0.1 pF and an active resistor network M_F-M_P of 3.54 MΩ and 1.42 kΩ, respectively, at the top-level design as shown in Figure 3. The circuit was designed with thick oxide transistors that allow a relatively high supply voltage of 3.3 V (VDD) in a standard 0.35 µm CMOS technology process. The achievable output rise time of the CSA circuit is given by $t_r = \frac{2.2}{2\pi GBW}$, where GBW is the gain bandwidth of the CSA core amplifier. From this formula, a fast pulse response of 7.36 ns was guaranteed for reaching 1 GHz bandwidth.

2.2. Analysis of the CSA Circuit

The first stage is a cascade topology developed based on a common source with diode-connected PMOS (M_2) so that the input is free from parasitic capacitance and the feedback amplifier controls the gate voltage.

Therefore, the CSA input becomes a virtual ground and the sensor capacitance is less significant to the CSA bandwidth. The specifications of the design impose to guarantee a high dc-gain and high stability. The overall transfer function of the small-signal model of the proposed circuit (Figure 4) is presented as follows:

$$A(s) = \frac{A_{OLDC}(1 + C_m(R_m + 1/g_{m3})s)}{\left(1 + \frac{g_{m3}g_{m7}r_{03}r_{o8}R_sC_m}{r_{03}+r_{o8}}s\right)\left(1 + C_m\frac{g_{m3}+g_{m7}}{g_{m3}g_{m7}}s + \frac{C_mC_L}{g_{m3}g_{m7}}s^2\right)} \quad (1)$$

where g_{mi}, r_{0i} and C_i are denoted as the equivalent transconductance, output resistance and the lumped capacitance at the ith gain stage. The output parasitic capacitance being lumped in the load capacitance C_L. The parasitic capacitances and parameter values of the circuit in Figure 4 was extracted during the implementation process and presented in Table 2.

$$\begin{cases} C_1 = C_{gd1} + C_{gd2} \\ C_2 = C_{gd3} + C_{gd8} + C_{gs7} \\ C_3 = C_{gd7} + C_{gd6} + C_L \end{cases} \quad (2)$$

Table 2. Design parameters of the proposed Front-End Electronics.

Transistor W/L(µm/µm)	gmk Value (µS)	Capacitance/λ
M1—62.5/10.5	gm1—61.4	C_L = 1 pF
M2—0.84/0.35	gm2—12.28	C_m = 50 fF
M3—18/0.35	gm3—50	C_F = 100 fF
M4,5,6—12/0.35	gm4,5,6—20	C_1 = 0.74 fF
M7—9/0.35	gm7—200	C_2 = 1.82 fF
M8,9—10/0.35	gm8,9—12	C_d = 534 fF
M_F—3/36	gm_F—13.13	C_i = 200 fF
M_P—2.772/0.7	gm_F—704.2	C_{L2} = 1 pF
M_d—2/23.6	gm_d—2.88	λ = 0.0746
M_i—10/41	gm_i—3.27	
M_{1sh}—3/20	gm_{ish}—4.67	
M_{2sh}—0.63/59.25	gm_{2sh}—0.467	
	$g_{03,08}$—0.1865	

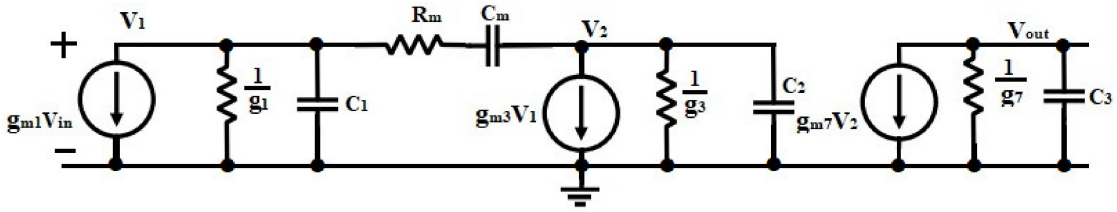


Figure 4. The small-signal model of the core Miller compensation with zero nulling resistors (MCNR) amplifier.

To study the stability of the design, the following assumptions are made to simplify the transfer function of the core amplifier. C_m and R_m being the Miller capacitor and the zero-nulling resistor, respectively, $C_3 \cong C_L \; and \; C_m$, $C_L >> C_1, C_2, g_{mi} \gg \frac{1}{r_{0i}}$; thus, (1) can be written as

$$A(s) = \frac{A_{OLDC}\left(1 + \frac{s}{\omega_{z1}}\right)}{\left(1 + \frac{s}{\omega_{po}}\right)\left(1 + \frac{1}{Q}\frac{s}{\omega_{p1}} + \frac{s^2}{\omega^2_{p1}}\right)} \tag{3}$$

where the associated parameters are given by (4)

$$\begin{cases} \omega_{z1} = \frac{g_{m3}}{C_m(1+R_m g_{m3})} \\ \omega_{po} = \frac{r_{03}+r_{o8}}{g_{m3}g_{m7}r_{03}r_{o8}R_s C_m} \\ \omega_{p1} = \sqrt{\frac{g_{m3}g_{m7}}{C_m C_L}} \\ A_{OLDC} = -\frac{g_{m1}g_{m3}g_{m7}r_{03}R_s}{g_{m2}(1+\lambda r_{03} I_{bias})} \\ Q = \frac{\sqrt{g_{m3}g_{m7}}}{(g_{m3}+g_{m7})}\sqrt{\frac{C_L}{C_m}} \end{cases} \tag{4}$$

However, the dc-gain (A_{OLDC}) of the circuit as depicted in (4) depends on I_{bias} and can be adjusted by an external resistor Rg; ˇ being the channel modulation parameter. (5) give the system's phase margin (PM) with pole-zero cancellation

$$PM = \tan^{-1}\left(\frac{GBW}{\omega_{z1}}\right) - \tan^{-1}\left(\frac{GBW/\omega_{po}}{Q\left(1 - \left(GBW/\omega_{po}\right)^2\right)}\right) \tag{5}$$

The proposed circuit has been simplified and analyzed based on the MATLAB development toolkit [19]. Small-signal parameters and parasitic capacitances of MOSFETs are used in the toolkit as input data to enhance the design of multi-stage Opamps (Figure 5). Illustrates the frequency response of an MCNR three-stage Opamp designed for 42° phase-margin (black line). It is evident that the amplifier exhibited two poles; the dominant pole ω_{po}, the large pole ω_{p1} and one zero, all associated with Equation (3). The poles are located at 74.6 kHz and 141.42 MHz, respectively, and the zero is situated at the frequency of 998 MHz. The feedback network is designed to introduce a phase lead near the crossover frequency, thus canceling the second pole of the Open-loop gain (OLG) which is located at the frequency of 141.42 MHz; then, increases the amplifier's phase margin. The transfer function associated with the feedback network is written as (6):

$$\begin{cases} K(s) = \frac{K(1+\tau_F s)}{(1+\tau_p s)} \\ \tau_F = R_F C_F \\ \tau_p = K\tau_F \\ K = \frac{R_P}{R_P+R_F} \end{cases} \tag{6}$$

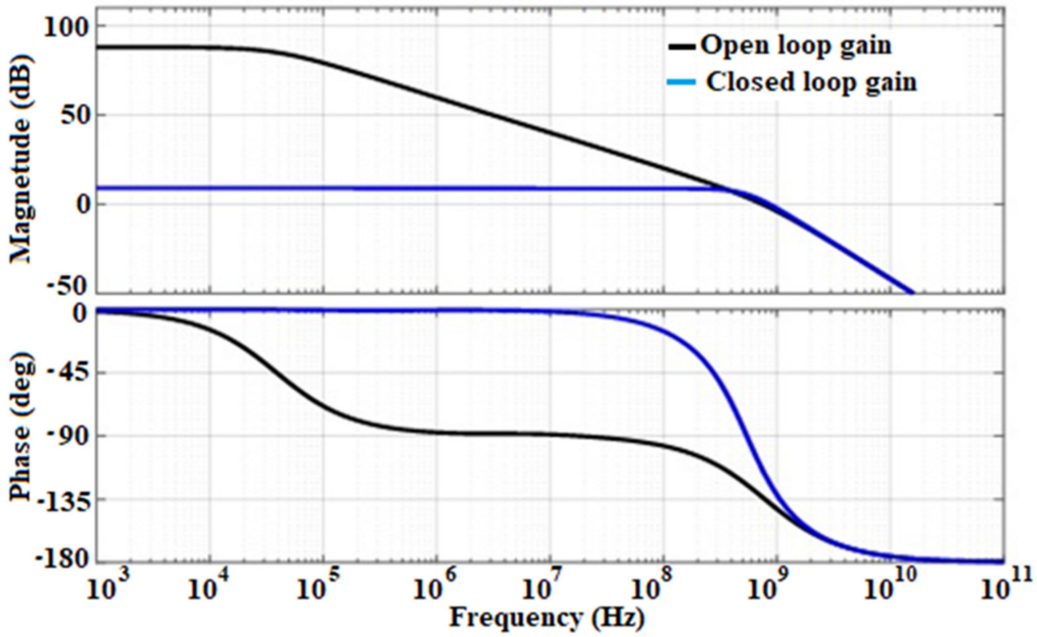


Figure 5. Graphical demonstration of the Open-loop gain (OLG) and Closed-loop gain (CLG) of the third-order system with a single-pole dominant pole.

As depicted in Figure 5, the Open-loop transfer function (OLTF) and Closed-loop transfer function (CLTF) are associated, respectively, with the Open-loop gain (OLG) and Closed-loop gain (CLG), the circuit should be designed to fit the requirements of this analysis. Therefore, rigorous transistor sizing and design should be implemented in order to achieve better performance, taking into account the parasitic effect and mismatch that generate noise in the device.

2.3. Feedback Lead Network (FLN) Implementation

This module comprises a charge collecting capacitor C_F and an active network resistor (MP and MF) based on a voltage-controlled NMOS resistor. The value of C_F was chosen to ensure sufficient high charge-gain conversion that will prevent the design against saturation. In fact, in most conventional CSA design, the charge gain is kept low enough to keep the preamplifier output from saturation. Since, the output saturation causes the ballistic deficit, which is a decrease in amplitude as the bandwidth has been degraded by the gain [35]. In this design, the bandwidth compensation is achieved thanks to the adjusted gain stage. Therefore, a feedback capacitor of 0.1 pF was set to handle a maximum input charge of 280 fC, without compromising the bandwidth. To minimize the feedback area, MP and MF are based on an NMOS transistor working in a linear region; their channel dimensions' ratios are sized to exhibit no parallel noise. However, It is a challenge to bias the feedback network because to achieve a large effective resistance, the operating region of the MOSFETs is of interest. Considering a MOS device biased in strong inversion and working in the linear region, the drain-source current characteristics can be written as (7):

$$I_{DS} = \mu_n C_{ox} R_d \left[(V_{GS} - V_{THN}) V_{DS} - \frac{{V_{DS}}^2}{2} \right] \tag{7}$$

Hence, M_P being biased to operate in the triode region, and neglecting the channel length modulation and the quadratic effect of the drain-source voltage, the equivalent resistor of the NMOS device is given as

$$R_{DS} = \frac{V_{DS}}{I_{DS}} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{THN})} \tag{8}$$

M_P is designed to handle 1.42 kΩ equivalent resistor with $\left(\frac{W}{L}\right)_P = \frac{2.772\ \mu}{0.7\ \mu}$. However, based on Equation (8), M_F was biased to operate in weak inversion moderate with $\left(\frac{W}{L}\right)_F = \frac{3\ \mu}{36\ \mu}$. This allows achieving a very large equivalent resistance of 3.542 MΩ.

2.4. Design of the CR-RC[1] Pulse Shaper

In order to tune the signal-to-noise ratio (SNR) of the sensor readout electronics and reduce the signal interference between signals from a different time, the output signal of the CSA is needed to be shaped using a first-order active CR-RC pulse shaper (PS) circuit as illustrated in Figure 6. Low-frequency noise (1/f) and thermal (high-frequency) noise was suppressed using a custom shaper circuit consisting of a differentiator and an integrator with constant time both equal to the optimal shaping time ($\tau_d = \tau_i = \tau_{s,opt}$). The pulse shaper circuit provides an output voltage proportional to the energy of the detected particles. The topology of the core amplifier used in the CSA is used for this purpose. Therefore, the loop gain A_{OL_SH} of the PS is given by (9) as follows:

$$A_{OL\_SH} = \frac{\Delta V_{CSA,max}}{\Delta Q_{max}} C_F \left(\frac{e}{n}\right)^n n! \quad (9)$$

where n is the order of the shaper. Using the design parameters allows achieving 2.67 loop gain. It is easy to derive the shaping design parameters as follows: $C_dR_d = C_iR_i$ and $\frac{R_d}{R_i} = \frac{C_d}{C_i} = \frac{1}{A_{OL\_SH}}$. For 200 fF integrating capacitor, $C_d = 534$ fF, $R_d = 400.75$ kΩ and $R_i = 1.07$ MΩ, respectively.

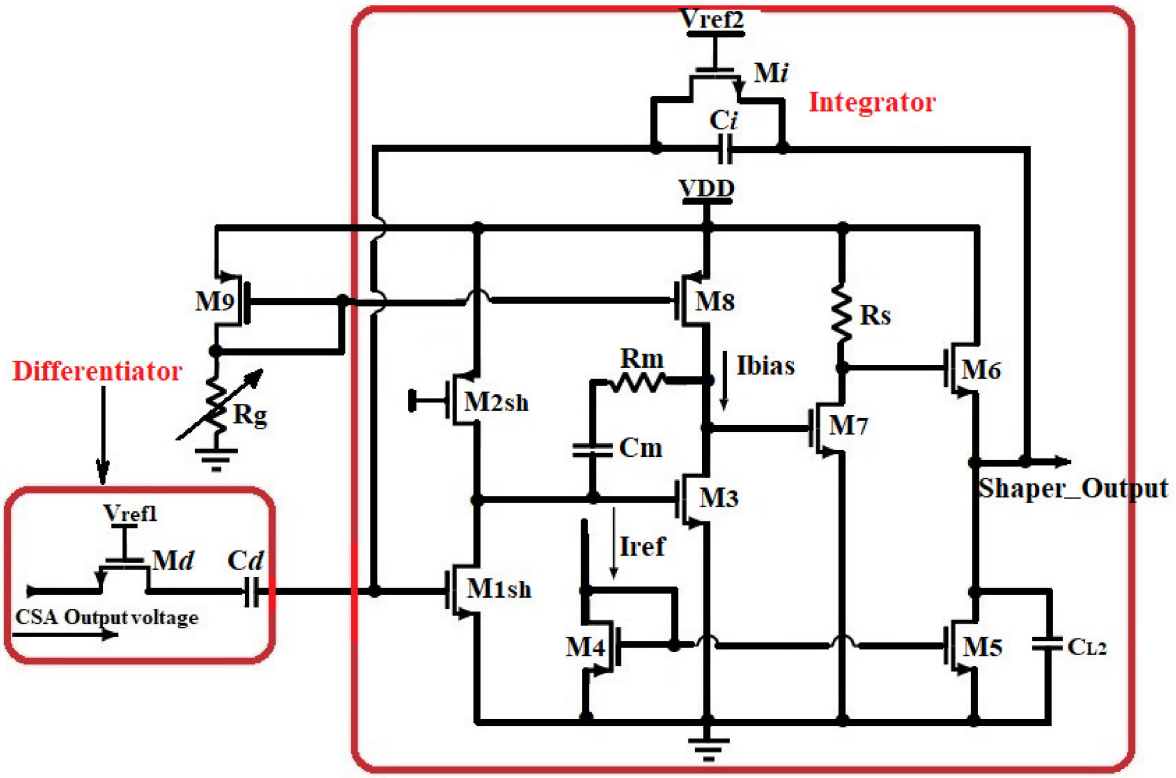


Figure 6. Schematic of the proposed structure of the Shaper.

Henceforth, R_d and R_i are very large, thus should occupy more space. Using (8) with suitable transistor biasing within the design process, the equivalent resistance can be derived from NMOS device operating in weak inversion moderate so that $\frac{W_i}{L_i} = \frac{10\ \mu}{41\ \mu}$, $V_{GSi} = 0.7$ V and $\frac{W_d}{L_d} = \frac{2\ \mu}{23.6\ \mu}$, $V_{GSd} = 0.9$ V. However, the PS core amplifier would exhibit

a gain-bandwidth given by $GBW_{SH} = \frac{1}{2\pi\tau_{s,opt}} = 744.1$ kHz. Hence, $GBW_{SH} = \frac{g_{m1\,sh}}{2\pi C_{L2}}$, g_{m1sh} being the transconductance of the input transistor and C_{L2} the total load capacitance of the shaper. For 1 pF, load capacitance, the small-signal transconductance is calculated from the previous expressions and controlled to be 4.67 µS, which allow simulating 912 nA drain-source current, exhibiting, therefore, the ultra-low-power dissipation of only 0.301 µW, while the geometric aspect ratio of the device was controlled at $\frac{W_{sh1}}{L_{sh1}} = \frac{3\ \mu}{20\ \mu}$. Moreover, the shaper input stage was chosen to be a common source with a P-channel MOSFET active load. The former device was biased to work in a strong inversion saturation regime by $V_b = 1.2$ V, and adjusted to handle $A_{OLSH} = -10$ input gain stage; so $g_{m2sh} = \frac{g_{m1sh}}{10}$. Despite the input transistors M_{1sh} and M_{2sh} which have been customized, the remained devices of the CSA core amplifier have been utilized to design the shaper module. The general parameters of the PS circuit are presented in Table 2.

2.5. Noise Optimization of the FEE Circuit

The sensors, preamplifiers and shapers are the main contributors to noises. The CSA, along with providing low-noise amplification, offers low input impedance (virtual ground) which stabilizes the potential of the sensor electrode and reduces the inter-electrode cross-talk [41]. The input transistor of the CSA is designed to operate in strong inversion saturation and optimized to handle the lowest possible ENC. The total ENC_{CSA} for a given feedback and sensor capacitor, according to the adopted CMOS process consist of three different components [6] and given as follows:

The most prominent thermal noise contribution can be calculated as (10):

$$ENC_{th}{}^2 = \frac{4K_BTn\gamma\alpha_n}{q^2}\frac{\left(C_{det} + C_f + C_g\right)^2}{g_m C_g}\frac{N_{th}}{\tau_s} \tag{10}$$

where K_B is the Boltzmann constant, T is the room temperature, η is the body factor, γ is the inversion factor, α_n the excess noise factor, N_{th} is the shaper noise index for the thermal noise, τ_s is the peaking time, C_{det} the sensor capacitance, C_f the feedback capacitor, C_g the gate capacitance and g_m is the input MOSFET transconductance.

The flicker noise also known as 1/f noise is expressed as (11):

$$ENC_{1/f}{}^2 = \frac{K_f}{q^2}\frac{\left(C_{det} + C_f + C_g\right)^2}{C_g}N_f \tag{11}$$

where K_f is the flicker noise coefficient and N_f the shaper noise index for flicker noise

The white parallel noise contribution due to the sensor leakage current (I_{leak}), the MOSFET gate current and feedback resistor R_f, is defined as follows (12):

$$ENC_i{}^2 = 2q(I_{leak} + I_G)N_i\tau_s + \frac{4K_BTN_i}{q^2R_f} \tag{12}$$

where q is the elementary charge, I_G the gate current of the input transistor, R_f the feedback resistance and N_i the shaper noise index for the white noise. In Equation (12), the first term refers to shot noise for a weak inversion MOSFET operation due to a higher potential barrier between source/drain and channel. However, the second term refers to the thermal noise generated by the very small potential barrier created by the positive gate potential in a strong inversion MOSFET [7,25].

Different components of the ENC were first optimized with respect to W and I_D, and then with respect to C_g [6] using the first-order shaper. The optimization technique well explained in refs. [6,33] is therefore adopted and the optimized parameters are derived as follows $W_{opt} = \frac{3\left(C_{det}+C_f\right)}{2C_{ox}L_{min}}$ and $I_{D,opt} = \frac{g_m{}^2L_{min}}{2\mu_nC_{ox}W_{opt}}$. The instability of the drain current (I_D) is established by the variation of charge in the depletion region, which constitutes the

channel width. L_{min} and W_{opt} are the minimal length and the optimal width of the input device. W_{opt}, being calculated at 62.5 µm and L_{min} = 10.5 µm the design requirements allow achieving very much less drain current of $I_{D,opt}$ = 2.5 µA, for the CSA input transistor. Since the bias current of M1 is fixed to its optimal value, increasing W/L reduces the overdrive voltage V_{GS}-V_{TH}, eventually driving the transistor in moderate or weak inversion. The threshold voltage variations were reduced based on conventional low-threshold voltage (LVT) operation, which consists of lowering channel doping, which narrows the channel depletion region, improves the subthreshold slope, and reduces the gate leakage contribution. Moreover, the V_{TH} optimization was implemented during the Spice simulations setting the bulk-source voltage of the inputs transistors to 0 (V_{BS} = 0 V). Moreover, while layout the design, mismatch reduction helps in reducing the fluctuation of V_{TH} taking into account the trade-off between drain-induced barrier lowering (DIBL) mitigation and gate leakage reduction [42]. Therefore, if the transistor works in this region, increasing its gate width too much worsens the noise, because it leads to more gate capacitance without improving the transconductance [6,41,43]. The total gate capacitance, which optimizes the different components of ENC, is obtained by solving the equations $\frac{\partial ENC_{th}{}^2}{\partial C_g} = 0$ and $\frac{\partial ENC_{1/f}{}^2}{\partial C_g} = 0$, respectively [6]. The solutions of those equations are found to be:

$$C_{g,th} = \frac{3}{2}\left(C_{det} + C_f\right) \text{ and } C_{g,1/f} = \left(C_{det} + C_f\right) \quad (13)$$

The values of the gate capacitances given by (13) limit the operating regime of the input device. The gate width is finally adjusted to achieve the matching condition defined in (13). At this point, if the contribution of the ENC due to flicker noise is greater than the one given by thermal noise, Cg can be further increased. Depending on the value of K_f and the peaking time, the optimization will result in a W yielding a gate capacitance between $\frac{3}{2}\left(C_{det} + C_f\right)$ and $\left(C_{det} + C_f\right)$. The input capacitance must also be much greater than the other capacitance sources connected to the input preamplifier in order to ensure that the sensitivity of the preamplifier is not compromised by external capacitance changes [25]. Considering the input transistor in the strong inversion saturation mode, W_{opt} leads to $C_{g,opt} = \left(C_{det} + C_f\right)$. Thus, in this regime, the same value of gate capacitance minimizes both flicker and thermal noise. Therefore, the total ENC of the CSA can be expressed as (14):

$$ENC_{CSA} = \frac{1}{q}\left(\left(\sqrt{\frac{A_1}{g_{m1}\tau_p}} + \sqrt{A_2}\right)\left(C_{det} + C_f\right) + \left(q(I_{leak} + I_G)\tau_s + \frac{4K_BT}{R_F}\right)N_i\right) \quad (14)$$

where $A_1 = \frac{K_B T n \gamma \alpha_n}{3} N_{th}$ and $A_2 = \frac{16 K_f N_f}{3}$.

However, the passive feedback resistance (R_f) is replaced by the voltage-controlled NMOS resistor network, which exhibited no parallel resistive noise. Moreover, the optimal shaping time is obtained by solving the equation $\frac{\partial ENC_{total}{}^2}{\partial \tau_p} = 0$. Thus (15) give optimal shaping time and (16) give the optimized ENC as

$$\tau_{s,opt} = \sqrt{\frac{A_1}{qI_{leak}g_{m1N_i}}}\left(C_{det} + C_f\right) \quad (15)$$

$$ENC_{CSA} = \frac{1}{q}\left(\left(\sqrt{\frac{A_1}{g_{m1}\tau_{s,opt}}} + \sqrt{A_2}\right)\left(C_{det} + C_f\right) + \left(q(I_{leak} + I_G)\tau_{s,opt} + \frac{4K_BT}{R_F}\right)N_i\right) \quad (16)$$

From analytical computation, it is clear that the minimum ENC of the CSA is achieved when τ_s =214 ns, which is the shaper constant time.

Assuming that the sharper module exhibits infinite gain and higher SNR, the impact of noise from its amplifiers can be reduced by increasing the size and power of the active devices [6,40]. The ENC contribution of the shaper comes from the dissipative feedback

component [6]. The parallel noise spectral can be stated as an equivalent parallel noise generator at the input of the charge amplifier by scaling it with the square of the charge gain of the shaper A_{OL_SH} [6,41,44,45]. Thus, the shaper ENC component is given as (17):

$$ENC_{SH}{}^2 = \frac{4K_BT}{A_{OL\_SH}{}^2 R_i} N_p \tau_s \quad (17)$$

where N_p is the ENC coefficient for white parallel noise [34].

The total ENC of the FEE, defined as the quadratic sum of the CSA and the shaper components can be expressed by (18) as follows:

$$ENC_{total} = \sqrt{\frac{1}{q^2}\left(\left(\sqrt{\frac{A_1}{g_{m1}\tau_{s,opt}}} + \sqrt{A_2}\right)\left(C_{det} + C_f\right) \right)^2 + \left(q(I_{leak} + I_G)\tau_{s,opt} + \frac{4K_BT}{R_F}\right)N_i + \frac{4K_BT}{A_{OL\_SH}{}^2 R_i} N_p \tau_{s,opt}} \; z \quad (18)$$

3. Simulation Outcomes and Discussions

3.1. Simulation and Implementation Framework

The performances of the proposed readout circuit were verified using LTSpice simulator and the layout was implemented in 0.35 µm CMOS technology process from TSMC, using Electric VLSI. For all the Spice simulations, the sensor was modeled by an ideal current source in parallel with capacitor C_{det} which values vary up to 2 pF. The Transistors were placed symmetrically, biased and designed by keeping the ratio $\frac{g_m}{I_D}$ sufficiently high in order to optimize mismatch along with the stability of other analog performance such as the gain-bandwidth product GBW [41,43]. The CSA input's transistor size and biasing current were optimized for matching the input capacitance to the target sensor's capacitance [26]. It was, therefore, biased with a low current of 2.5 µA supplied from 3.3 V (VDD). The shaper's core is based on a common source input stage with a P-channel MOSFET active load, biased to work in a strong inversion saturation regime with $V_b = 1.2$ V. This allowed simulating 912 nA drain-source current, exhibiting, therefore, an ultra-low-power dissipation of only 0.301 µW and achieving the GBW of 744.1 kHz. Its peaking time was configured optimizing the overall ENC of the FEE and controlled at 214 ns.

3.2. Results and Discussions

The specifications and design parameters of the proposed front-end electronics were improved as compared to recently published works. Figure 7 shows the influence of the bias current on the open-loop gain of the core amplifier. As illustrated in that figure, is possible to increase the dc-gain of the device just by adjusting I_{bias} value, for a feedback loop of R_F = 3.542 MΩ and C_F = 0.1 pF. To achieve suitable amplification of the CSA, I_{bias} was controlled to 2.5 µA by an external resistor (Rg) as mentioned in the previous section. Frequency analysis swept from 1 kHz to 10 GHz and is displayed in decade form. The bias current is adjusted by changing the value of the external resistor Rg that allows changing the transconductance of M8, and therefore increasing the dc-gain of the Opamp as depicted in Equation (4). Figure 7. shows the Spice simulation results of the open-loop gain (OLG) of the Opamp versus the I_{bias} current. It is evident that for the low value of I_{bias}, wide GBW is achieved but involves poor stability of the circuit. The simulated results show that the core amplifier achieved a 2.5 µA bias current, a unity gain-bandwidth of 997.84 MHz with a 42° phase margin. The very little difference with the analytical value is due to the parasitic and the residual noise generated by the circuit. However, the phase margin remains poor and the circuit behaves unstable. Therefore, the bias current is a crucial parameter that may guarantee high dc-gain, the stability of the circuit need to be compensated. Since the GBW is stabilized through the dc-gain, it should be necessary to keep the highest possible phase margin for maintaining signal integrity [23,24,46]. Therefore, its feedback network determines the closed-loop gain (CLG) stability of the design. Since the sensor, the capacitance was set to 2 pF and the extracted parasitic capacitor of the input transistor was around 20 fF; the total input capacitor was fixed to 2.02 pF. Nevertheless, a resistor has a parasitic capacitance and a capacitance has a parasitic resistance. Thus, an RC feedback

network (R_F-C_F) models the feedback circuit. Loop-gain stability has been tested during the charge vs voltage conversion when R_F-C_F is bypassed [21]. The Opamp equivalent load capacitors are also taken into consideration by varying C_F. For achieving the highest stability of the circuit, the closed-loop gain is adjusted by the R_F-C_F sizing. The feedback equivalent resistor (R_F) was implemented by associating the drain-source resistance of two N-channel MOSFETs (M_F and M_p on Figure 3) device biased to be in the triode strong inversion region. Under this condition, the parallel noise was minimized to a large extent; thus, the circuit is stable and continuously sensitive and can be maintained in this condition without adjustment for spectroscopy purposes [16,40,41,43]. Thus, with that technique, we achieved up to 3.542 MΩ feedback equivalent resistances, which guarantee a phase margin of 82°. The closed-loop gain of the design is shown in Figure 8. As depicted on that plot, the maximum unity bandwidth (GBW) achieved by the design (for stability conditions) is controlled at 1 GHz, which is a bit different from the one obtained in the open-loop condition. Thus, the feedback compensation circuit and the parasitic capacitance of the design produce an error estimated at 0.216% on the GBW. The difference between the analytical model is just 0.016%. This little difference is because the analytical solution was computed with ideal components, neglecting, therefore, some internal capacitance and mismatch produced by the devices. Adjusting I_{bias} as shown in Figure 7, enhances the phase margin and the bandwidth could be extended to more than 2 GHz. The compensation capacitor brings together a pole and zero into the loop equation. The zero always occurs before the pole because of $R_F > R(M_F)||R(M_p)$. The zero is placed to cancel out the first pole along with its associated phase shift. The analytical closed-loop transfer function shown in Figure 5 (blue line), was confirmed by the Spice simulation results in Figure 8. When the τ_F zero is placed at ω_{p1}, it cancels out the pole (p1) causing the Bode plot to continue on a slope of −20 dB/decade. When the frequency gets to $\omega_F = 1/R_F C_F$, this pole changes the slope to −40 dB/decade. The phase shift is canceled before the second op-amp pole occurs, and the circuit reacts as if the pole was never introduced. The benefit of pole-zero cancellation is improved pulse shape and resolution in the energy at a high counting rate [4,23,25,32].

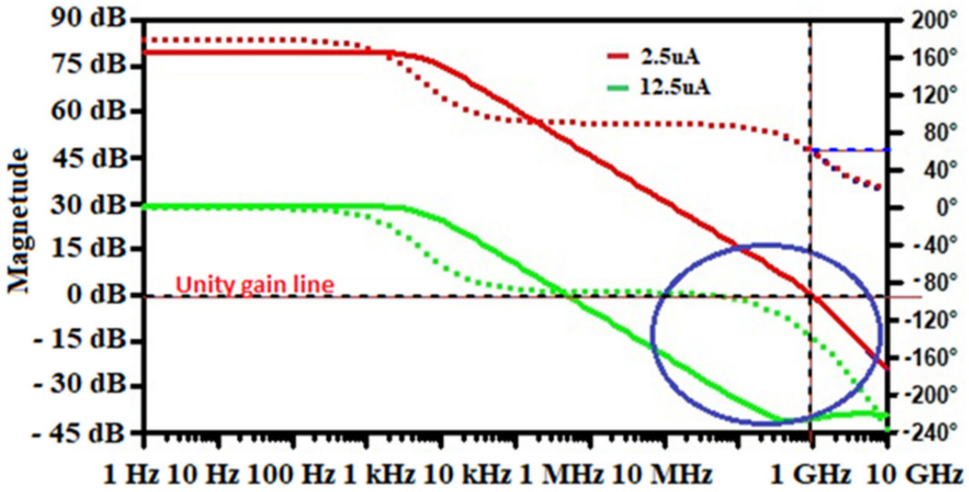


Figure 7. Influence of bias current (I_{bias}) on the Open-loop gain.

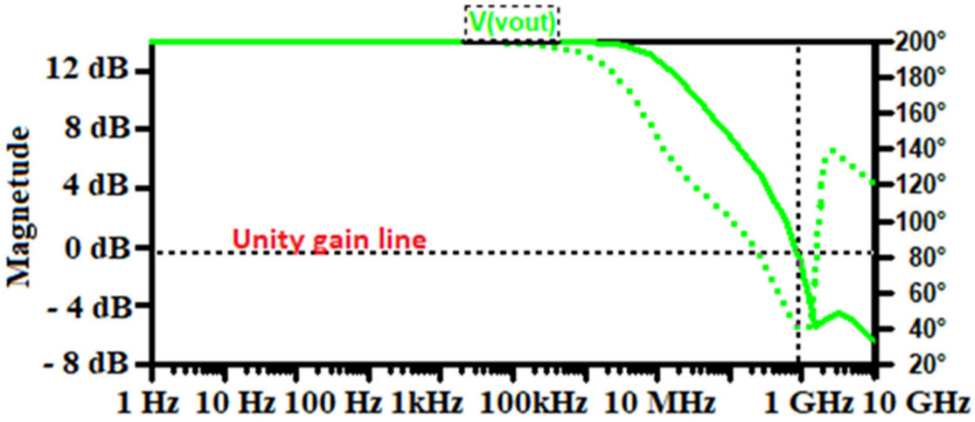


Figure 8. Bandwidth compensation using feedback lead network-based a MOSFET resistor; which allows achieving high stability.

The noise corner frequency fc, which is the frequency at which the asymptotes of the flicker and thermal noise components cross was identified as the frequency range over which the CSA op-amp noise is dominated by either the 1/f or the thermal noise components [36–49]. In agreement with this definition [36], the noise corner frequency of our design has been controlled to be 652.9 MHz. Therefore, the Input-referred-noise (IRN) of the circuit was plotted in Figure 9, in the frequency range of 600 MHz to 4 GHz. The IRN spectral density extracted is 5.23 nV/$\sqrt{}$Hz at 997.82 MHz. Moreover, when developing analog front-end recording (AFE), a lower IRN guarantees the signal quality [16] of the recorded neuron activity and low power consumption can prolong the existence of the implanted recording system in the human body [6,36]. However, in the CSA, the parameter that embodies the noise performance is the ENC, namely the input charge necessary to get at the output a signal equal to noise. Its calculation was based on this intrinsic definition, neglecting the standard calculation depending on the post-CSA circuit, not present in this design [33,34,36]. Equations (18) and (19) have been computed to provide optimal design parameters; an optimum shaping time of 214 ns has been extracted and the overhead ENC has been controlled at 37.35 e-with a sensor capacitance of 0 pF and a slope of 16.32 e-/pF worsened the noise; while the Spice simulations provided a noise slope factor of 19.58 e-/pF. The ENC as a function of I_D and W has been computed and presented in Figure 10. It is clear that the thermal noise is decreased when an increase in the input transistor current occurs but it comes up with the increase in the bandwidth over which the thermal noise is integrated as well. Therefore, those effects canceling each other out. Hence, significant reductions in power consumption are achievable with little or no noise penalty if the device is made to operate at a low count rate [46–48]. Moreover, the reduction in the bias current of the input transistor offers good separation between the preamplifier rise and fall time [17,48,50,51]. According to Equation (19), we can note that, at short peaking times, the noise increases rapidly with capacitance and increases as the peaking time is reduced. For Si-PIN diodes, the capacitance scales with area, so large area sensors exhibit more noise [12,37,38].

For SDDs, the capacitance is much lower and nearly independent of area. This noise is only weakly dependent on temperature [12,37,43]. At long peaking times, the noise increases with peaking times (Figure 11) and with leakage current. Since leakage current increases exponentially with temperature, reducing temperature helps dramatically.

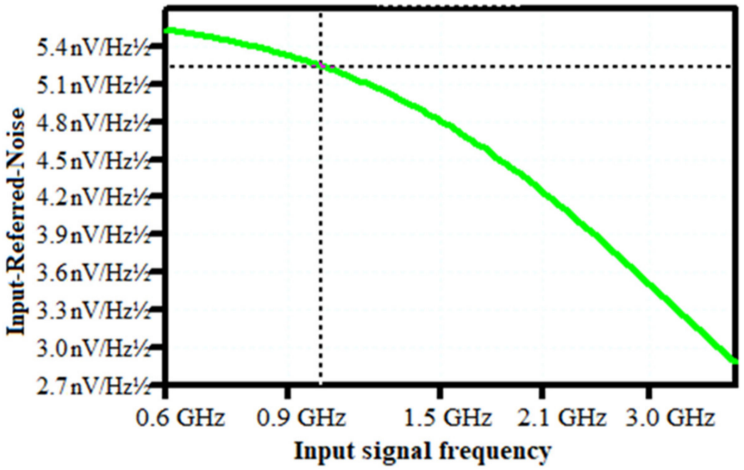


Figure 9. CSA Input-Referred Noise.

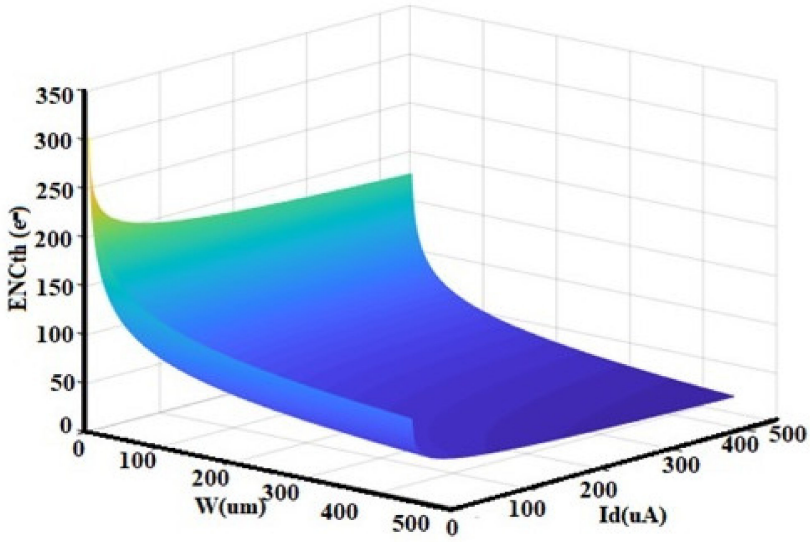


Figure 10. ENCth as a function of W and drain current (Id) [6].

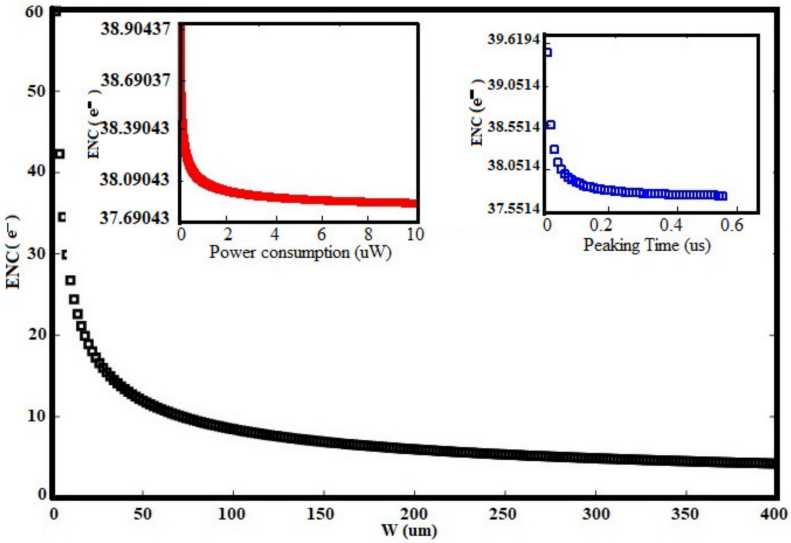


Figure 11. Equivalent Noise Charge (ENC) as a function of W.

There will be always some peaking time at which the noise is minimum, where the delta and step terms are equal. There is no advantage for operating at a longer shaping time, because of the integration of more parallel noise during this period. The optimum time constant is shorter for lower capacitance and longer for low leakage currents. Otherwise, the third term of Equation (14) represents the shot noise (due to the leakage current of the sensor) which could be considered to be 10 nA (for the worst silicon sensor) while performing the total noise of the intrinsic CSA circuit (Figure 11). The intrinsic noise represents the noise of the preamplifier without any sensor connected. The ENC varies from 39.0437 e^-r.m.s to 37.5643 e^-r.m.s as the peaking time is changed from 10 ns to 0.5 µs. From the spice simulations, it is shown in Figure 11 that, the ENC is reduced when the power dissipation increases. The ENC achieves a value of 37.69043 e^-rms when the power dissipation is larger than 8.56 µW. This means that the specification of the power dissipation satisfies the design requirements. As shown in Figure 12a–d, the design consideration taken to optimize the total ENC for the used techniques is also used to choose the optimal Id and W, as a trade-off between ENCth specification of the peaking time and power consumption [4,16,25]. Those optimal parameters were Id = 2.5 µA and Wopt = 62.5 µm which corresponds to gm = 61.4 µS. An optimal transistor channel length Lmin = 10.5 µm was chosen to minimize the input capacitance of the CSA circuit, therefore. Especially on Figure 12a,b), it is evident that ENC_{th} has a minimum value at Wopt, and that value has a low dependency on Id and τ_s, respectively. From those two graphs, it is clear that above 62.5 µm the noise improvement with the drain current and the peaking time increasing, respectively, is very low. The same observations are made in Figure 12c where the dependency of the ENCth is very low above 2.5 µA.

The transient responses of the readout circuit are shown in Figures 13 and 14. Different charges of width 1 ns were injected into the sensor. The output swing of the CSA achieves up to 1.962 V peak and decreases slowly thereafter because of the feedback action. The fall time of the signal is about 300 ns, setting by C_F and R_F. It is evident in Figures 14 and 15 that the CSA output is amplified and shaped; for 200 fC-injected charges, the shaper output swing achieved the peak value of 4.16 V after 241.8 ns peaking time.

The input charge dynamic range of the FEE is from 0 fC to 280 fC. The output voltage linearly increases with the increase of input charges, the charge-to-voltage gain from the output node of the CSA, the CR-RC shaper, is provided by simulation outcomes as, 546.56 mV/MeV (9.92 mV/fC) and 920.66 mV/MeV (16.7 mV/fC), respectively, using the equivalence from mV/fC to mV/MeV as mentioned in ref. [52]. The output voltage range of the Shaper is 22 mV to 4.16 V. The overall gain of the readout module can be adjusted by the feedback capacitance of the CSA.

Figure 13 shows the effects of the CSA gain bandwidth on the ENC_{th}, with different input transistor widths. It is readily recognized that the lower transistor width leads to higher thermal noise for GBW from 1 to 20 dB. This is because, for lower GBW, the collection process is slowed down; due to the highest rise time, the thermal noise accumulated in the device increases accordingly. This results in the attenuation of the output swing and therefore a poor energy resolution [4,25,34]. As depicted in Figure 13, the optimal input transistor width (62.5 µm), is the critical value for which the variation of the thermal noise is not sensitive to the CSA gain bandwidth. Therefore, from a point of view of minimizing the ENCth, a typical gate width is needed at a higher GBW [4,25]. From a practical point of view, higher GBW leads to a short rise time than a very fast collection process. So, instead of the wide bandwidth of the CSA, the noise accumulation process is very brief due to the shortest collection time (7.36 ns) [5]. Accordingly, the optimal input noise matching results in an optimum input device aspect ratio. The smallest transistor size should be therefore taken at the expense of some system resolution [4,25,34]. However, the output stage of the shaper being an N-channel source follower will help in reducing the non-linearity of the device for the large output signal. The nonlinearity of the readout module was controlled at only 0.8% and 1.24%, respectively, for the CSA and shaper, provided by the spice simulation results.

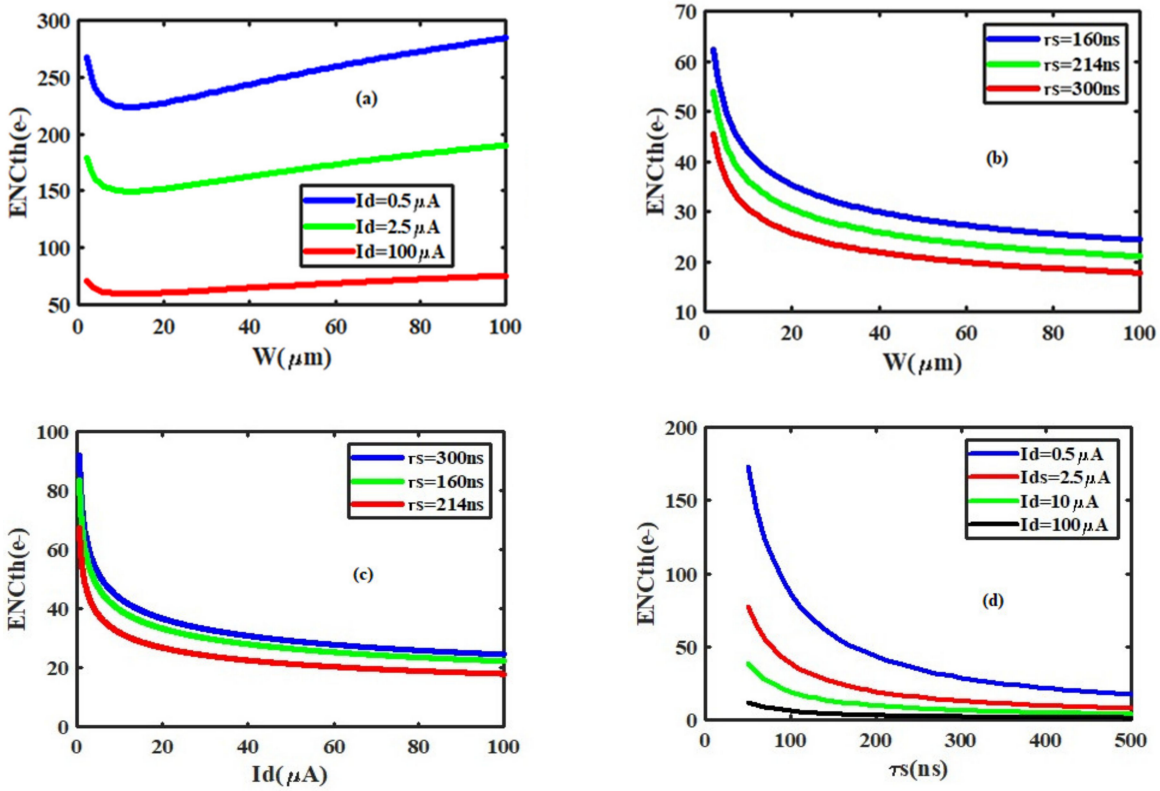


Figure 12. ENCth versus different design parameters: (**a**) as a function of W for different sets of the input device drain current; (**b**) as a function of W for different sets of the shaping time; (**c**) as a function of the input device drain current for various peaking time; (**d**) versus the peaking time for different sets of the input transistor drain current.

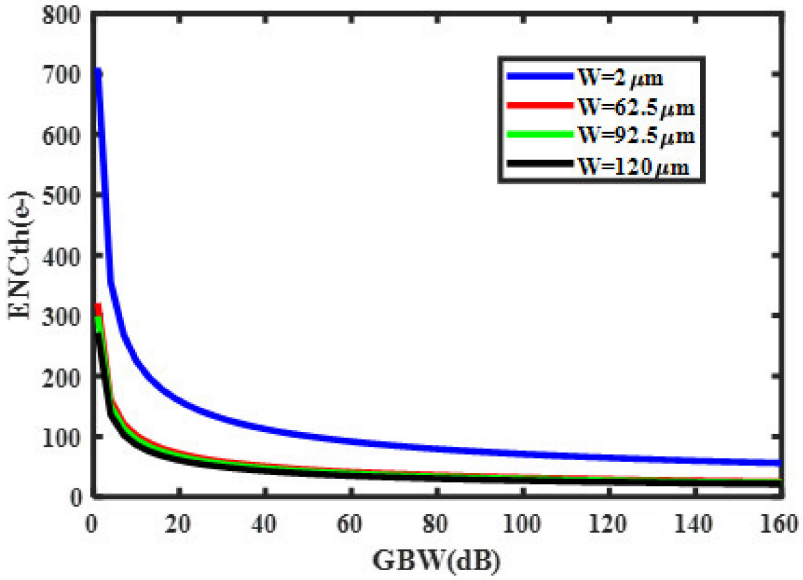


Figure 13. Effect of the CSA gain bandwidth (GBW) on ENCth for the different input gate widths.

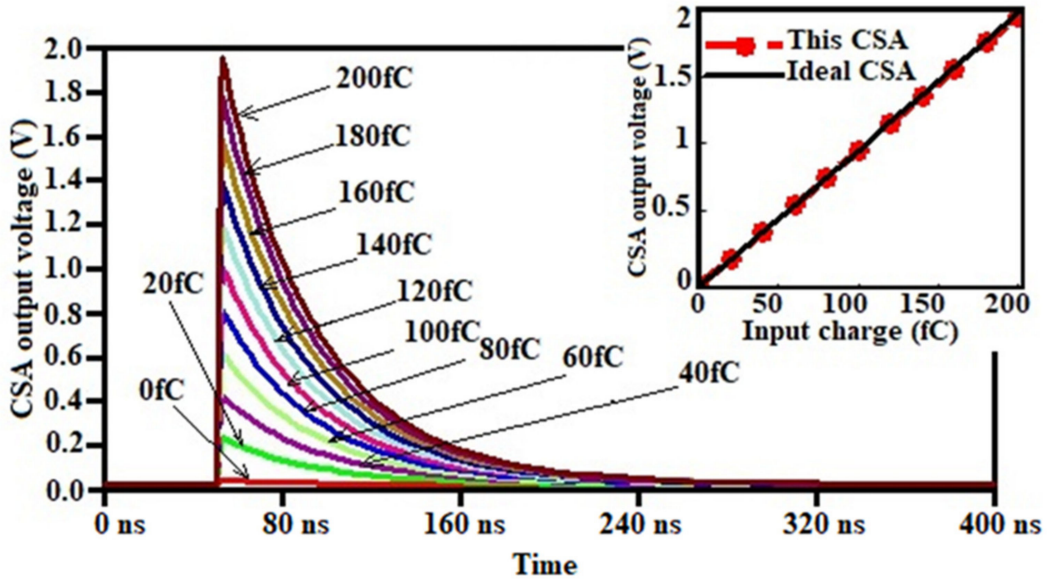


Figure 14. CSA output voltage for different input charge.

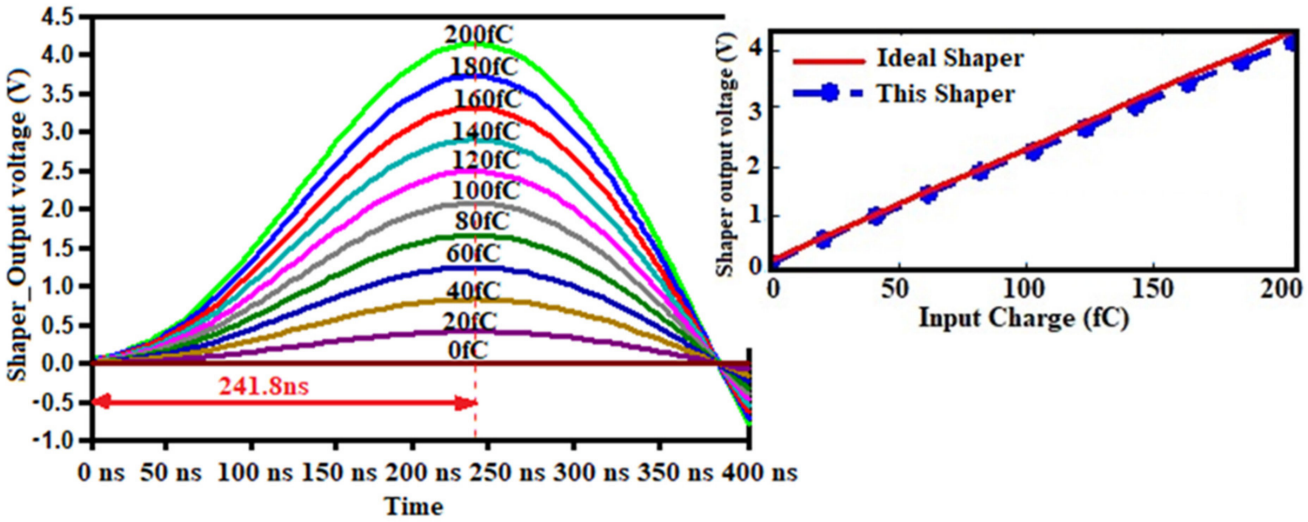


Figure 15. Pulse shaper (PS) output voltage for different input charge.

The capacity of the circuit to operate under high particle flux and high charge production rate was simulated and presented in Figure 16. The sensor with 2 pF capacitance was set to handle 1000 radiation events. Up to 280 fC charges were therefore injected at preamplifier input with 1 fC maximum step. The output swing of the circuit was computed and the histogram of the amplitude was therefore generated.

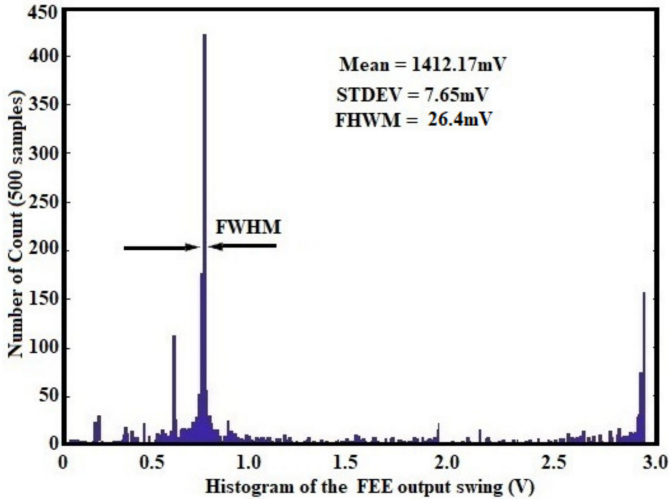


Figure 16. Histogram of output voltage for high charge production rate.

3.3. Post Layout Monte Carlo Simulation Results

Power-efficiency and robustness of the proposed circuit against process variation were performed through a post-layout Monte Carlo simulation. As illustrated in Figure 16, this histogram describes the response function of the proposed FEE against several radiation events. This corresponds to the histogram of the energy of the detected particles (or injected charges) in real-time operations [6,8,37,47]. Two important observations can be made. On the one hand, the output swing (offset voltage) for 0 fC is very low and is about 22 mV. This means that the proposed FEE does not exhibit high input offset; this confirms the zero dc-voltage components shown in Figures 14 and 15 for different input charges. The radiation-hardened behavior of our proposed front-end has been achieved thanks to input transistor sizing which helps in keeping lower gate capacitance and optimal transistor width for a considerable reduction in electric noise [9,12]. On the other hand, the proposed design is capable of handling up to 280 fC without losing the integrity of the signal (preserving the information of interest). So, exhibited a wide input charge range. The mean output swing of the design was controlled at 1412.17 mV with a 7.65 mV standard deviation. The full-width half-maximum (FWHM) was only 12.23 mV and contributed only at ~1.87% of the output swing. Since the circuit energy response is illustrated by Figure 16, the lowest percentage of the FWHM is satisfactory and confirms that the proposed FEE can handle high-energy resolution [12,16] for spectroscopic applications. In Figure 17 the post layout Mont Carlo simulation results, highlighting the ultra-low power behavior of our circuit is presented. The average power consumption of the design was controlled at 8.72 μW while exhibiting only 1.83 μW of standard deviation. From this analysis, it can be concluded that, the power dissipation of the proposed front-end does not vary significantly due to process variations.

Figure 18 shows the histograms of conversion gain based Monte Carlo simulation results of the proposed front-end circuit for 500 runs, which exhibited the histogram of the conversion gain for both the CSA circuit and the PS module, for 10 fC charge injected at the input of the sensor. The highest sensitivity of the design is then achieved; for a week amount of injected charge the histograms of the conversion gain observed on Figure 18a,b show a mean value of 589.4 mV/MeV, and a standard deviation of 90.36 mV/MeV for the CSA stage while the shaper circuit exhibited 872.73 mV/MeV mean value and 95.86 mV/MeV standard deviation. This shows that the outcomes got with Monte Carlo models do not vary fundamentally for 500 runs and the front-end performance is very steady and robust. The less difference of those parameters with the spice simulation results is attributed to the parasitic capacitance obtained while designing the feedback circuits of the different stages. This can be compensated by adjusting the feedback capacitance of the CSA or increasing the loop gain of the shaper via an external device.

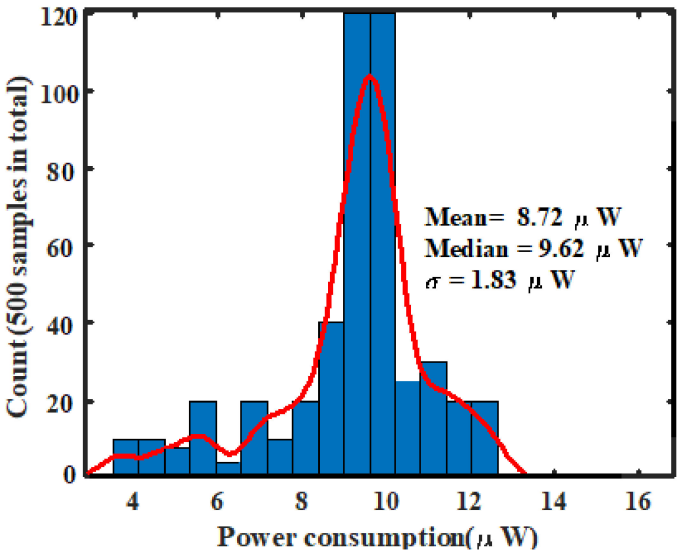


Figure 17. Histogram of power consumption against process variation.

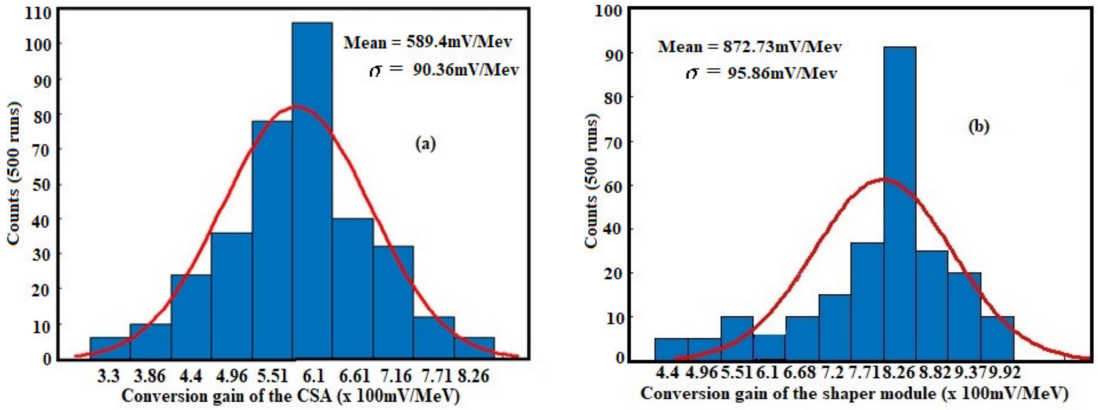


Figure 18. Histograms of the conversion gain for both (**a**) the CSA and (**b**) the PS.

Moreover, as highlighted in Figure 19, the ENC and shaping time are extracted from the post-layout simulation results and plotted for different values of power consumption. The system achieved an ENC of 37.6 e^- at 214 ns peaking time while dissipating only 8.72 µW of power from 3.3 V supply voltage. At 241.8 ns peaking time, the proposed front-end exhibited an ENC of 38 e^-, while consuming very less power of 10.14 µW. Those relatively low variations of equivalent noise charge and power consumption provided by the post-layout simulation at 241.8 ns peaking time, do not differ so much from those provided by the spice simulations; confirming, therefore, the ultra-low-power and low-noise behavior of our design.

The total core layout area occupied by the proposed readout electronics is sized at (256.2 × 80) μm^2 as shown in Figure 20. Parasitic extraction was used to extract the netlist with parasitic. The voltage supply is 3.3 V; the maximum power consumption achieved through post-layout simulations is about 8.72 µW for the whole circuit, which is 1.83% higher than that provided by the spice simulations. This little increase in power dissipation is mostly due to the parasitic and mismatch while laying out the design [11,17,49]. In this research, the gain-bandwidth product of the circuit was stabilized by means of a high-frequency feedback loop, which operates according to the voltage-controlled NMOS resistor (R_F and Rp) technique [6,22]. The innovation of the proposed FEE results in the implementation of the external bandwidth compensation based gain stage, which allows achieving high gain with less amount of current, preventing, therefore, the pulse

height degradation along with bandwidth limitation and power dissipation. Further, the combination of the Miller compensation with the Feedback lead network is used to raise the best PM and guarantee decent stability of the gain-bandwidth product with good linearity for high-energy resolution applications.

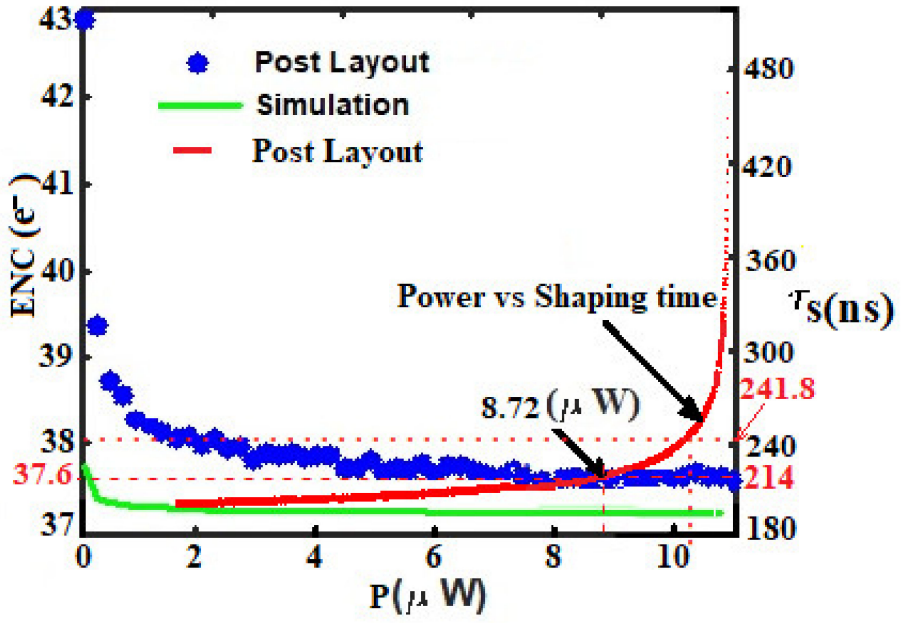


Figure 19. Validation of the design performance in terms of ENC, power consumption, and shaping time.

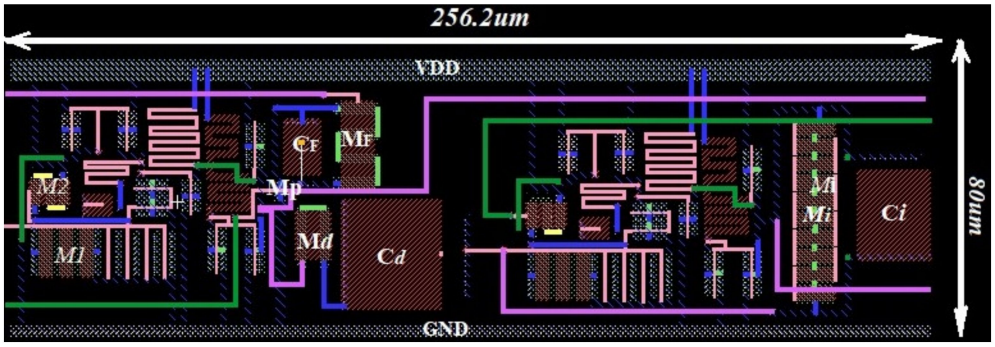


Figure 20. Core layout of the proposed readout FEE.

As a rundown, in Table 3 the general highlights of the FEE circuit are presented. To achieve a high signal-to-noise ratio (SNR) and reduce power consumption, ENC, and active die area of the chip, the configurations presented in the literature have been consulted [6,14,16,20,22,24,39,52–56]. Considering the critical contrast on the input transistor's capacitance, the outcomes are empowering. Therefore, readout electronics performances are in agreement with the state-of-art specifications. On the one hand, the design of the input and feedback transistors allowed achieving high linearity, with high phase margin and sufficient low noise to ensure good stability. On the other hand, the optimization of I_{bias} helps in adjusting the dc-gain of the CSA circuit and avoids saturation, which affects the linearity and the energy resolution of the device. Therefore, the adjusting gain stage allows achieving a high-energy resolution with wide gain bandwidth (1 GHz) and the operational amplifier stability has been guaranteed with 82° phase margin and 88 dB minimum DC-gain. A figure of merit (FOM) must be agreed upon for comparison with previous research works.

Table 3. Performance comparison of the proposed Front-End Electronics.

Parameters	This Work	[26]	[49]	[45]	[17]	[22]
CMOS Technology	0.35 µm	0.18 µm	0.35 µm	0.13 µm	0.35 µm	0.18 µm
Power Supply	3.3 V	1.8 V	±1.65 V	1.2 V	3.3 V	1.8 V
Power Consumption	8.72 µW	8.7 mW	2.1 mW	4.8 mW	–	2.1 µW
Input Parasitic Capacitance	0.2–2 pF	0.1 pF	17 pF	5 pF	10 pF	-
Gain/Operating Bandwidth	88 dB/1 GHz	–/9.1 GHz	—	-	60 dB/5.1 kHz	-
ENC	37.6 e^- + 16.32 e^- /pF	278.2 e^- + 26.6 e^-/pF	58.4 e^- + 12.7 e^-/pF	600 e^- + 100 e^-/pF	650 e^-	-
Amplifier Gain (mV/MeV)	546.56/920.66	513.67/1740.2	9366.45	550.96	826.45	0.044
Active area (mm^2)	0.0205	0.093	47.64	0.7225	0.75	0.038
Input Dynamic	0–280 fC	0–15 fC	6 fC	0–60 fC	80 fC	450 pC
Peaking time	214 ns	40 ns/250 ns	500 ns/2 us	100 ns	—	—
Figure of merit (FOM) (MHz/µW)	116.82	1.05	–	0.002	-	14.29

The following FOM was defined to highlight the performances of this design with recently published works [53–56]. This parameter can be explained as the speed-sensitivity product to the power dissipation for a given sensor capacitance. The higher the FOM, the lower the white noise at lower power dissipation [55].

$$FOM = \frac{f_t}{P_d} \text{ (MHz/µW)} \quad (19)$$

where P_d is the power dissipation and f_t being the preamplifier transition frequency. From Table 3, the proposed front-end electronics exhibited a quite high and acceptable FOM of 116.82 MHz/µW. The circuits presented in refs [17,26,49] exhibit higher conversion-gain than that of our design, but they suffer both from higher ENC and low input dynamic. The circuit in ref. [22] has a higher input dynamic of 450 pC and consumes only 2.1 µW of power, but suffers from a very low conversion factor of only 0.044 mV/MeV, involving poor FOM of only 14.29 MHz/µW.

3.4. Process Variations

Process variations outcomes worsen with reducing the channel length [52,53]. Mismatch being a function of threshold voltage (VTH) and supply voltage (VDD), low VTH (LVT) transistors have a reduced mismatch impact due to higher VDD/VTH ratio than standard VTH (SVT) or high VTH (HVT) transistors; the proportionate change in temperature from SVT to HVT is much larger as compared to that from LVT to SVT [54,56,57]. Thus, it is more advantageous to move from HVT transistors to SVT devices, but this results in high power dissipation. Large MOS devices increase the intrinsic parasitic capacitances, which leads to more thermal noise, but also reduces local head transfer and mismatch for LVT that can increase the power consumed by the design [52,53,55]. In order to reduce the influence of the high threshold voltage, the input transistors of both the CSA and the pulse shaper modules have been optimized based on conventional LVT operations [57]. In fact, LVT devices have a higher current density and transconductance than regular threshold voltage (RVT) transistors for the same bias conditions, which enforces the previous suitable applications, commented [58,59]. Furthermore, LVT transistors have higher transconductance efficiency, so for low power applications, LVT MOSFETS are recommended. RVT devices have lower VDSsat than LVT MOSFETs. The fact that for applications that need lower supply voltages and do not need require high gains RVT devices are a good choice [58,59]. In addition, LVT transistors present slightly lower parasitic capacitances than RVT transistors, which involves that LVT devices are more suitable for high-frequency applications than the RVT [58–60]. Taking into account the trade-off between transistor size and mismatch, we perform optimal transistor sizing/matching with a parallel arrangement of the devices to reduce the parasitic and mismatch effects, canceling, therefore, the short circuit power generated by those parasitic [53,55,60] and achieved 8.72 µW of maximum power consumption.

4. Conclusions

Design techniques of a low-noise, stable and ultra-low power FEE for silicon sensors applications have been described in this research. The design consisted of a compact CSA module linked to a one-order fast PS. The proposed structure was described and analyzed to handle the optimal design parameters. The Spice simulations were therefore implemented and validated by post-layout simulations and Monte Carlo results in 0.35 µm CMOS process, and the specification parameters confirmed the theoretical model. As per FEE design requirements, the input stage transistor aspect ratio has been optimized to guarantee the possible low noise performance. An adjusting gain stage was implemented in the preamplifier stage to control the loop gain and compensated, therefore, the bandwidth limitation of the core amplifier. The feedback resistors were implemented using an active MOS device based voltage-controlled resistor; this allows canceling the parallel noise contribution in the CSA, reducing the energy loss in the shaper feedback capacitance and achieving an amplitude resolution of 1.87% FWHM therefore. The CSA and shaping module achieved a charge to a voltage conversion factor of 546.56 mV/MeV and 920.66 mV/MeV, respectively, verified by the Monte Carlo simulation results, and it is therefore compatible with the state-of-the-art. With a supply voltage of 3.3 V, the readout circuit consumes a maximum power of 8.72 µW and occupied a very low die area of 0.0205 mm^2. The theoretical analyses together with the post-layout simulations allowed us to prove the functionalities and performance metric of the proposed front-end for ultra-low power and low-noise ROIC for pixel-strip sensors.

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ORIGINAL RESEARCH PAPER

A low-offset low-power and high-speed dynamic latch comparator with a preamplifier-enhanced stage

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Abstract

The preamplifier module is a crucial element while designing dynamic latch comparators. The traditional double tail comparator utilizes a differential pair as the preamplifier stage. The circuit is generally suffered from high power dissipation and low comparison speed. This research reports the design and implementation of a low-offset, low-power and high-speed dynamic latch comparator. In this work, an enhanced differential pair amplifier is employed in the preamplifier stage, to improve the power dissipation and the comparison speed of the device. A custom latch structure with rigorous transistor sizing was implemented to avoid short circuit current and mismatch in the module. The effective trans-conductance of the cross-coupled transistors of the latch was therefore improved for an optimal time delay solution. The equation associated with the delay was derived and the parameters that embody the speed were identified. The design has been validated by corner analysis and post-layout simulation results in 65 nm CMOS technology process, which reveals that the proposed circuit can operate at a higher clock frequency of 20 GHz with a low-offset of 4.45 mV and 14.28 ps propagation delay, while dissipating only 67.8 μW power consumption from 1 V supply and exhibited lowest PDP of 0.968 fJ. Moreover, the core circuit layout occupies only 183.3 μm^2.

1 | INTRODUCTION

The advent of CMOS technology with the miniaturization of MOS transistors sizes allows increasing the capabilities of mixed-mode signal circuits for storing and processing a very big amount of data. Thereby increasing the speed of data processing systems. Generally the signals to be processed are analogue and must therefore be converted into a digital format. Requiring therefore, the utilization of analogue-to-digital converters (ADCs). Due to the increased usage of mixed-signal circuits in a variety of systems such as video systems, wireless communications, Ethernet and health-care systems, the demand for high-speed and low-power ADCs are increasing. Specification of mixed-mode signal circuits heavily relies upon the use of technology [1–4]. With the improvement of CMOS technologies, the supply voltage and the input voltage full-scale range decrease while the threshold voltage off the MOSFET is not scaled down at the same rate as technology. Moreover, mismatch and process variations increase dwindling feature size when devices are also scaled down [1,3,4]. However, device size combined with supply voltage reduction is an important aspect while designing high performance and accurate ADCs. One of the crucial mixed-mode parts circuits of the ADC and most sigma-delta modulators greatly affected by the technology process is the comparator. The development of high-speed and power-efficient sigma-delta ADC has speeded

up the demand of high speed and low-power comparators [1,2,5].

Comparator is the crucial element while designing high-speed data transmission circuits as ADC, since it controls the performance and the accuracy of the device. To empower the performances of such a device, the comparator needs to be power-efficient and exhibited low-noise, high resolution and high-speed. Therefore, high-performance comparators are necessary to amplifier a big output voltage. Consequently, a faster and accurate comparator involves high gain and high bandwidth [5–7]. Thus, for high speed and low-power applications, latch comparators are used instead of static comparators. Because they provide positive feedback, and therefore, charging of output node is faster as compared to the static comparator [8].

The static power dissipation of the Latch-type voltage sense amplifier is inconvenient with scaled-down of transistor sizing [9]. However, due to the several stacked transistors, a high voltage headroom is required for proper operation, which is not appropriate with scaled CMOS technology. The speed and offset of this structure is highly sensitive to input common-mode voltage [10], which is not appropriate for application with input common-mode variation. So, for high-performance design, the positive feedback stage of the latch should be moved away from the inputs.

Recent studies are drawn to design double tail comparator, since it has less stacking transistors, which make it suitable for low voltage, low-power and high-speed applications [9,11]. The amplification and latch stage are separated each other, which enables it to employ low tail current in the former and high current in the latter leading to low offset and high-speed respectively [9,12]. But, increasing the speed and reducing power dissipation, the offset and kickback noise are increased. These are a major concern while designing dynamic latched comparator (DLC). However, a low offset requires, larger transistors; this occupied more area by enlarging the parasitic capacitances, slowing the regeneration process and increasing the power dissipation [10,11,13]. The characteristics of an accurate dynamic latch comparator are defined by its input-referred offset voltage for a given power dissipation, speed and die area.

This paper reports the design of a traditional double tail comparator in terms of time delay and input referred offset. A compact architecture is therefore proposed in order to improve the delay and offset voltage due to kickback noise in the conventional topology. The circuit utilizes the enhancement NMOS load, which reduces the output swing and improves the power consumption and the comparison speed of the circuit. To avoid parallel oscillations and short circuit power dissipation in the latch stage, the cross-coupled transistors consisting that block was isolated to ground state, a suitable transistor sizing was performed during the design process. Therefore, the mismatch and parasitic capacitance were reduced and the trans-conductance of the cross-coupled transistors was improved. An output buffer was adopted in the last stage, in order to filter the residual noise coming from the latch. Detailed analysis of the time delay and power dissipation of the whole circuit has been discussed and compared to state-of-art architectures; a method is therefore proposed to reduce the total delay and the power consumption of the traditional double-tail comparator. That empowered the design and makes the proposed architecture compact for handling low-offset, low-power and very high-speed operations. The design was validated by the Process-Voltage-Temperature (PVT) analysis and post-layout simulation results, implemented in 65 nm CMOS technology process from TSCM using Electric VLSI.

The rest of this paper is organized as follows. Section 2 presents the conventional double-tail comparator (CDTC) and the analysis related to its operating mode and time delay. In Section 3, the proposed dynamic latch comparator is presented; analysis related to its operating mode, power consumption, kickback noise and time delay was discussed and then compared with the one in Section 2. The design considerations are then applied, validated, discussed and compared to previous works in Section 4. The paper has been summarized in Section 5.

2 | CONVENTIONAL DOUBLE-TAIL COMPARATOR

A CDTC is shown in Figure 1. This topology has less tacking compared to the traditional dynamic comparator (single-tail comparator). The double tail enables both a large current in the decision stage and wider M_{tail2}, for fast latching independent of the input common-mode voltage (Vcm), and a small current in the input stage (small M_{tail1}), for low offset [14,15]. The operation of this comparator is as follows. During the reset phase (CLK = 0, M_{tail1} and M_{tail2} are off), transistors M3-M4 pre-charge F2 and F1 nodes to V_{DD}, which in turn causes transistors MR1 and MR2 to discharge the output nodes to ground. During decision-making phase (CLK = V_{DD}, M_{tail1} and M_{tail2} turn on), M3-M4 turn off and voltages at nodes F2 and F1 start to drop with the rate defined by $I_{\text{tail1}}C_{F(1,2)}$ and on top of this, an input-dependent differential voltage $\Delta V(F1, F2)$ will build up. This voltage is transferred on to the latch circuit by transistors MR1 and MR2. Latch regeneration starts once the nodes voltage F1 and F2 are not sufficient for MR1 and MR2 to hold output to zero. Therefore, for V(Inp) > V(Inm), Outp is pulled to V_{DD} and Outm to ground as shown in Figure 2. The double-tail topology is suitable for low-voltage applications due to less stacking; kickback noise should be normally reduced due to the effective shielding of input and output by MR1 and MR2 [16,17], which will enable to handle high-speed and low-offset operations. However, transistors M7 and M8 consisting the cross-coupled inverter are not isolated to the ground state, when the clock rate is very high, there is a period that nodes F2 and F1 pull MR1/MR2 to reach sufficient voltage that may turn it on; at the same time, MR1/MR2 and the corresponding cross-coupled device operating in the regeneration phase, acts as in parallel. That involves parasitic oscillation caused by parallel MOSFETs, which results in a poor reduction of kickback noise in the circuit. Parallel MOSFETs are extremely susceptible to oscillation during switching transitions when there is an imbalance in the current

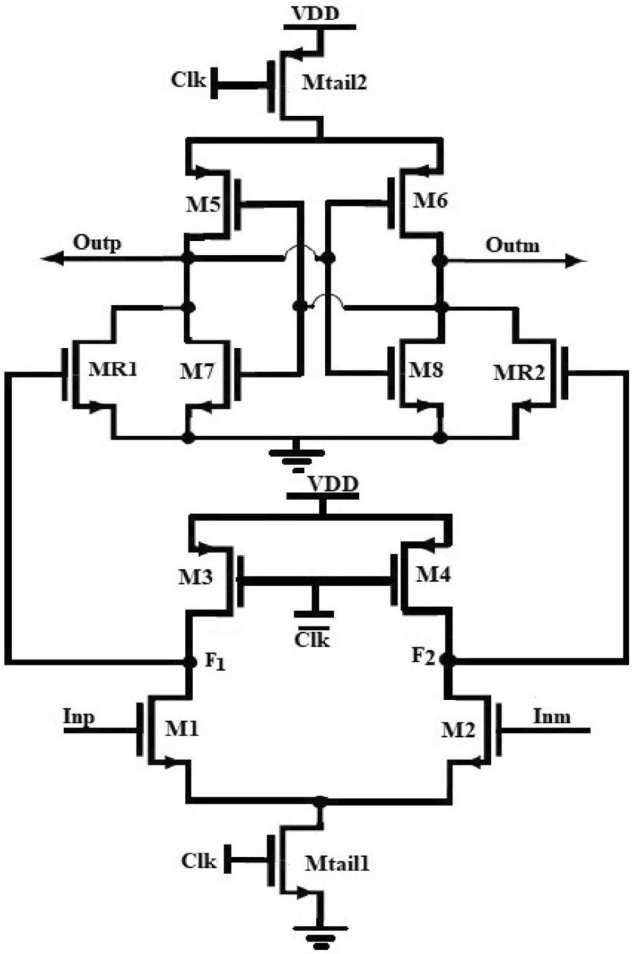

FIGURE 1 Block diagram of conventional double-tail dynamic comparator

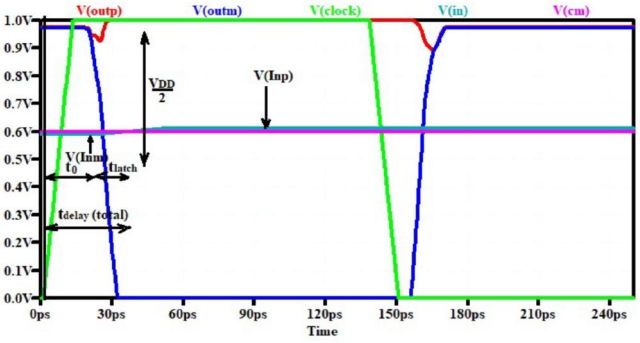

FIGURE 2 Transient simulation of the conventional dynamic latch comparator (V_{DD} = 1 V, V_{cm} = 0.5 V, ΔV_{in} = 5 mV, clk = 20 GHz)

sharing. Moreover, the slow dropping rate of F1 or F2 nodes in the pre-charge mode leads to a significant imbalance between MR1 and MR2, and then produces a significant dynamic offset, since MR1 and MR2 drains are directly connected to the latch output nodes. Therefore, isolating those transistors to the latch output nodes would help in lowering the offset. The delay of the comparator is defined as the time that the output

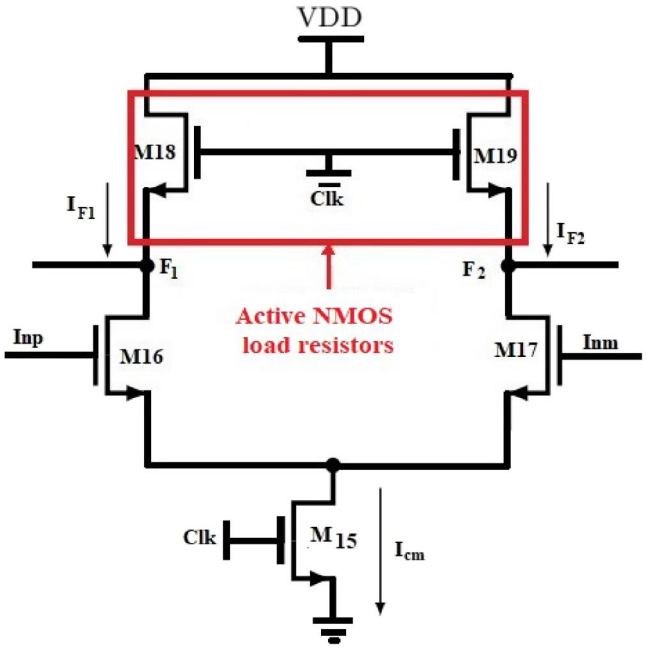

FIGURE 3 Block diagram of proposed preamplifier with enhancement NMOS load

difference takes place to reach $\frac{V_{DD}}{2}$. The total delay of the comparator is composed of latch delay, caused by cross-coupled inverters (M5/M6, M7/M8) and the delay occurred to charge output load capacitance until the first NMOS transistor (M7/M8) turns on [11,18]. Figure 2, shows the time response of the CDTC with a very small differential input voltage of 5 mV.

The analytical expression of the total delay of the conventional double tail comparator can be written as:

$$t_{delay} = t_0 + t_{latch} \tag{1}$$

$$t_0 = \frac{V_{THN} C_{out}}{I_P} = \frac{2 V_{THN} C_{out} \mu_p C_{ox} \frac{W_P}{L_P}}{g_{mP}^2} \tag{2}$$

where C_{ox} is the gate oxide capacitance, μ_p the hole mobility, V_{THN} is the threshold voltage of M7 and M8, C_{out} is the load capacitance of the output nodes, I_P is the current that passes through M5, g_{mP} is the transconductance of the PMOS transistor M5; W_P and L_P are the channel width and length of M5, respectively. However, the total effective transconductance ($g_{m,\mathrm{eff}}$) of the inverter consisting of M5 and M8 and is defined as follow:

$$g_{m,eff} = g_{mP} + g_{mN} \tag{3}$$

where g_{mN} is the trans-conductance of the NMOS device of the inverter. Since the NMOS transistor M8 is off during this period, g_{mN} is negligible. Therefore, t_0 being the period from the rising edge of the clock to the time when Outp and Outm are charged to V_{THN} considered in Ref. [14].

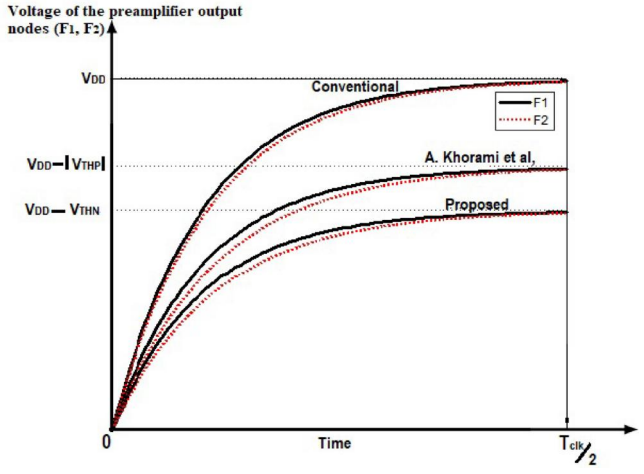

FIGURE 4 Voltage at the preamplifier output nodes during the evaluation phase for both the proposed, conventional and Ref. [21] topologies

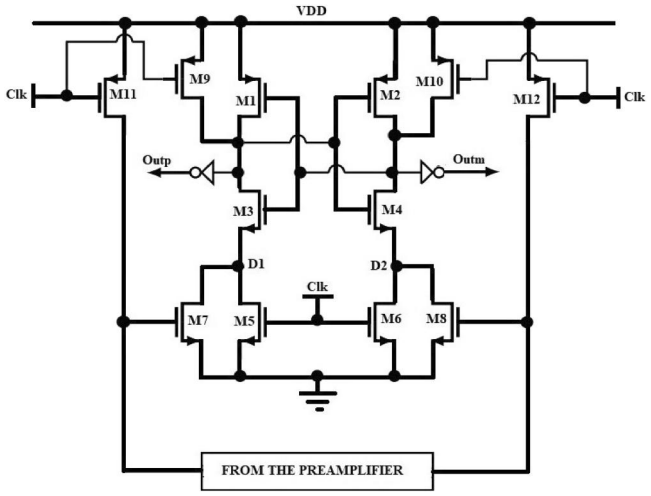

FIGURE 5 Block diagram of the proposed dynamic latch comparator

$$t_0 \simeq \frac{V_{THN}C_{out}}{I_P} = \frac{2V_{THN}C_{out}\mu_p C_{ox}\frac{W_P}{L_p}}{g_{mP}^2} \tag{4}$$

However, the time delay of the latch is given by Equation (5) as follow:

$$t_{latch} = \frac{C_{out}}{g_{m,eff}} \ln\left(\frac{\frac{V_{DD}}{2}}{\Delta V_0}\right) \tag{5}$$

where $\Delta V_{out} = \frac{V_{DD}}{2}$ and ΔV_0 is the difference of the initial output voltage of the latch at the beginning of the regeneration process. Since all the transistors of the cross-coupled inverter are ON during the evaluation process, the total effective trans-conductance is calculated as follow:

$$g_{m,eff} = C_{ox}\frac{W_P}{L_P}(\mu_P(|V_{GSP}| - V_{THP}) + \mu_N(|V_{GSN}| - V_{THN})) \tag{6}$$

Therefore, the total time delay of the conventional double-tail dynamic latch comparator can be expressed as:

$$t_{delay} = \frac{2V_{THN}C_{out}\mu_p C_{ox}\frac{W_P}{L_p}}{g_{mP}^2} + \frac{C_{out}}{g_{m,eff}} \ln\left(\frac{\frac{V_{DD}}{2}}{\Delta V_0}\right) \tag{7}$$

As illustrated in Equation (7), the delay strongly depends on the differential input voltage, the capacitive load of the output nodes of the latch and the trans-conductance (gm) of the input and intermediate transistors. Increasing ΔV_0 results in reducing the delay. At the end, once the decision is completed, both the intermediate transistors (MR1 and MR2) cut-off; since the node F1 and F2 discharge to the ground [11,18], there is no contribution to improve the effective trans-conductance of the latch. Therefore, enhancing the effective trans-conductance of the inverter will help in optimizing the total delay of the comparator; and then increasing the speed of the device.

3 | PROPOSED DYNAMIC LATCH COMPARATOR

The proposed dynamic latch comparator utilizes a differential pair amplifier with the enhancement-NMOS load to achieve sufficient gain for low offset and high-speed solution as depicted in Figure 3. Therefore, the gain of this comparator will be high due to using the enhanced differential amplifier, which leads to improving the power consumption and the comparison speed [11,19]. The NMOS load transistor's source swing from 0 to $V_{\mathrm{DD}}-V_{\mathrm{THN}}$ when its gate and drain are clocked from 0 to V_{DD}; comparing to the PMOS counterpart in which nodes swing from 0 to V_{DD}. So, the differential output nodes (F1 and F2) should be pre-charged from 0 to $V_{DD} - V_{THN}$ Figure 4. Furthermore, For NMOS, the V_{TH} is increased when its body–source voltage is biased to be negative. This is referred to as reverse body biasing [19]. Besides, transistor M15 is sized so that its on-resistance allows the enhanced differential pair to be biased near the weak inversion at the start of the evaluation phase. When clock is high (Clk = VDD), the enhanced differential pair starts a specific tail current (I_{cm}). The large finite resistance of M15 produces an increasing $\frac{g_m}{I_D}$ aspect ratio with decreasing V_{GS}. The variability of V_{THP} and V_{THN} (in PMOS and NMOS transistors) tends to be quite high in nano-metre CMOS technologies [20]. Thus, it must be kept as low as possible through proper transistor sizing to reduce the body effect which lowers the voltage swing at the preamplifier output nodes. The whole circuit works into two phases: reset or pre-charge phase and regeneration or Evaluation phase.

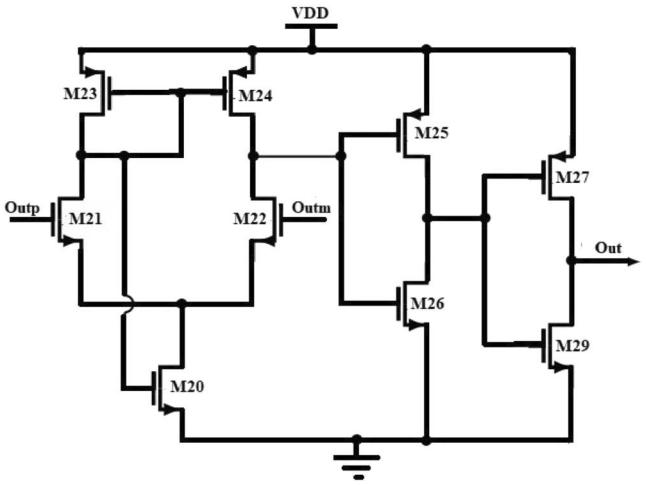

FIGURE 6 Block diagram of the output buffer of the proposed dynamic latch comparator

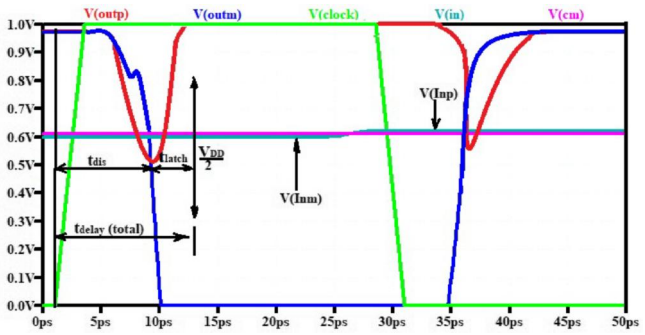

FIGURE 7 Transient simulation of the proposed dynamic latch comparator (V_{DD} = 1 V, V_{cm} = 0.5 V, ΔV_{in} = 5 mV, clk = 20 GHz)

3.1 | The reset phase or pre-charge

In the reset phase, the clock is low; the tail transistor of the sense amplifier (M15) is off. Therefore, the current source of M15 is switched off; ensuring that there is no static power consumption in the first phase. Nevertheless, M19 and M18 are ON, pulling terminal F1 and F2 $V_{DD}-V_{THN}$ to. As a result, M7 and M8 turn ON. Since M5 and M6 are off; M7 and M8 ON; nodes D1 and D2 are discharged to ground. The pull-up transistors (M9 and M10) of the latch as shown in Figure 5, are ON so, the output nodes Outp and Outm are pre-charged to V_{DD}.

3.2 | The evaluation phase

M19, M18, M9, M10, M11 and M12 are Off. Therefore, M4 and M3 begin to conduct. Since Vinp > Vinm, the drain voltage of M16 started to fall at a faster rate than the drain of M17 due to the highest trans-conductance of M16 comparing to M17. The tail transistor of the sense amplifier is ON and begins to conduct. Therefore, the positive feedback from the cross-coupled M2, M3 kicks in; the node D1 drops faster and pulls Voutm to low logic; therefore, M2 turns ON and pulls Voutp to high logic. Ones the decision made, comparator outputs control M4 and M3, which will be turn off to avoid static power dissipation. The opposite effect occurs when Vinm > Vinp; in that case Voutp is pulled to low logic and Voutm to high logic.

To reduce the kickback noise due to the transient at the regeneration nodes D1 and D2, the drains of the transistors forming the input differential pair need to be isolated from the regeneration nodes during the regeneration phase. This is done using switching transistors M7 and M8 between the regeneration node and the drains of the input differential pair. Those switches which are biased to work in strong inversion, are sized to exhibit high trans-conductance for thermal noise prevention. Thus, isolating the regeneration node and the drains of the input differential pair when regeneration starts. However, offset voltage is reduced using custom transistor sizing/matching during the design process, to avoid mismatch and process variation.

Transient simulations showing the outputs settling to inputs that are very close to the trip points of the latch circuit are given in Figure 6. Suitable transistor sizing/matching was performed to obtain very small offset voltage at the input common mode voltage of 0.5 V. As depicted on that figure, the comparator will become very slow and its outputs may not settle to a valid level. The differential input voltage is set to 5 mV, that value is very small and closed to the offset voltage, this affects the time response of the circuit which enters in a metastable state. Meta-stability is a problem that occurs in all latching comparators when the input is near the comparator decision point. That phenomenon is mostly due to parasitic; the interconnects between the transistors and the bulk silicon include a lot of parasitic capacitances. Those capacitances, particularly at the nodes with the positive feedback of the latch (M2, M3), are seriously influencing meta-stability and the regeneration process. To avoid that, we used a symmetrical placement of all the transistors while laying-out the design [22], the Enhancement NMOS load in the preamplifier stage, and all the other NMOS transistors of the circuit were designed to handle a zero potential between the source and substrate. This will reduce to a great extent the source-substrate parasitic capacitance and therefore lowering the probability of having meta-stabilities.

3.3 | Power dissipation

For low-noise and energy efficiency requirements, the weak inversion model was adopted for the transistors in Figure 3. Transistors were biased and designed by keeping the ratio $\frac{g_m}{I_D}$ sufficiently high to optimize mismatch along with other analogue performance such as the gain-bandwidth product GBW [23]. Since moving from strong to weak inversion and from a design perspective (i.e. constant current), two balancing phenomena occur: the mismatch increases for a given transistor size but decreases with increasing transistors surface [24,25]. So using high $\frac{g_m}{I_D}$ is obviously of high interest for low-

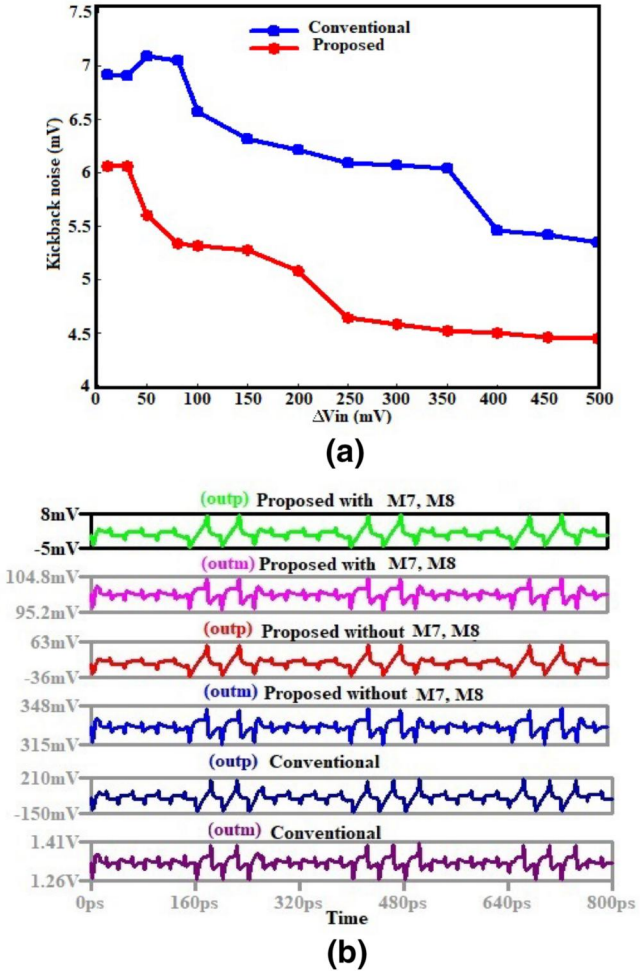

FIGURE 8 Kickback noise error on the comparators output voltage versus differential input voltage (a) and Transient simulation showing the Kickback noise error at the comparator outputs for both the conventional double-tail comparator and the proposed circuit in the absence & presence of M7, M8 transistors (b) $\Delta V_{in} = 20$ mV

voltage and low-power applications [25]. The output common-mode voltage of the preamplifier discharges by $\Delta V_{Fi,cm}$ from the pre-charge to V_{DD}, with an average discharge current I_{cm} and during integration time T_{int}. Therefore, the common-mode voltage drop at the preamplifier output nodes is defined as:

$$\Delta V_{Fi,cm} = \frac{I_{cm} T_{int}}{C_L} \tag{8}$$

Power consumption is optimized based on load transistor modelling and the time variance of the preamplifier output nodes. The average power of the supply voltage during one period of the comparison is obtained from the well-known formula [21],

$$P_{total}(t) = \frac{1}{T_{clk}} \int_0^{T_{Clk}} V_{DD}(I_{cm}).dt \tag{9}$$

where,

$$I_{cm} = I_{F1} + I_{F2} \tag{10}$$

Since the NMOS load transistor's source swing to $V_{DD}-V_{THN}$ when it gate and drain are biased by V_{DD}, the differential output nodes (F_1 and F_2) should be pre-charged from 0 to $V_{DD}-V_{THN}$. Considering the threshold voltages of MOS devices provided by the Predictive Technology Model website in 65 nm CMOS process ($V_{DD}-V_{THN} < V_{DD} - V_{THP}$), using the NMOS load device would help in lowering the preamplifier power consumption. However, the power consumption of the latch is negligible compared to the power consumption of the preamplifier [21]. Therefore, the total power dissipated in the design can be derived as follow:

$$P_{total} = \frac{2C_L V_{DD}(V_{DD} - V_{THN})}{T_{clk}} \tag{11}$$

Based on Equation (11), the percentage of power reduction increases by a factor α is given by Equation (12).

Considering the average of the typical value in 65 nm CMOS technology, the power reduction is around 42%. By using the NMOS load instead of the PMOS counterpart, a factor of 6% of the total power dissipation is saved from comparing to Ref. [14].

$$\alpha = 100 \times \frac{V_{THN}}{V_{DD}} \tag{12}$$

3.4 | Kickback noise

When the regeneration phase starts, the switch opens and the two cross-coupled inverters implement positive feedback; this makes the output voltages go towards 0 and V_{DD}, according to the small output voltage found at the end of the reset phase. Besides, the effects of the internal capacitances of the MOS devices and local mismatch on transistors can exacerbate the situation [26]. The input voltage is disturbed, which may degrade the accuracy of the converter. This disturbance is usually called kickback noise. Generally, high-speed and high power-efficient comparators generate more kickback noise [27,28]. Figure 7a shows the peak output voltage error as function of ΔV_{in} for both the conventional and the proposed comparator. It can be observed that increasing ΔV_{in} result in lowering the noise effect in our design. In fact, at the pre-charged phase, the input differential voltage is applied and amplified, while the regeneration process not yet started, no disturbance occurs [10]. At the beginning of the comparison phase, these auxiliary transistors

are turned on and help the circuit to start the decision-making and then the regeneration process [1,26]. Also, those transistors which are in the triode region are parallel with input differential pair transistors and help in keeping the drain of the input transistors to sense a less voltage variation, which leads to less kickback noise [1,28] as depicted on Figure 7b. On that figure, the kickback noise error at the comparator outputs is simulated in the absence and in the presence of M7, M8 devices and is compared to that produced by the CDTC for 20 mV differential input voltage ($\Delta V_{\text{in}} = 20$ mV) during the reset-to-regeneration transition. The proposed comparator exhibited low kickback noise due to using the auxiliary transistors M7, and M8 to isolate the preamplifier output nodes first, and secondly reducing mismatch effect and parasitic capacitance of the transistors while designing the devices. Therefore, the offset reduction in the feedback loop consisted of suitable transistor sizing operating in the weak inversion region and mismatch optimization [25,29].

3.5 | Thermal noise

The proposed enhanced differential pair which devices operate in weak inversion mode exhibited high gain, provided by $g_{m16,17}$. There is a possible increase of input noise at the differential input therefore [1]. During the evaluation phase, M19, M18, M9, M10, M11 and M12 are Off; so do not contribute to the noise behaviour of the proposed circuit. However, M1-M4 devices are cascaded, so their noise effect is negligible at low frequencies [1]. Thus, the total input referred noise voltage of the comparator consists of M5-M8, M16/M17 noise contribution. M16/M17 devices are sized identically to produce the same/similar input referred offset [30]. The input referred noise of those devices consisting the input differential amplifier for weak inversion operation is well analysed in Ref. [30] and given at a time $t = T_{int}$ as:

$$v^2_{n,th,in}(T_{int}) = \frac{2nkT}{C_L.\Delta V_{Fi,cm}(T_{int}).\left(\frac{g_{m16,17}}{I_{cm}}\right)_{T_{int}}} \tag{13}$$

where, n, is a process constant, $I_{\text{cm}}(t)$ is the tail current, T_{int} the integration time, k the Boltzmann constant and T is Kelvin's temperature.

Moreover, M7-M8 can be seen as complementary input which thermal noise can be modelled as a voltage source in series with the input. Thus, exploiting the analysis given in Ref. [1], the thermal noise contribution of M5-M8 at the output of the comparator is given as:

$$V^2_{n,th,out}(T_{int}) = \left(I^2_{n,5,th} + I^2_{n,6,th} + I^2_{n,7,th} + I^2_{n,8,th}\right)\left(R^2_{out}\right) = 8kT\gamma\left(g_{m5,6} + g_{m7,8}\right)R^2_{out} \tag{14}$$

where, γ is the channel thermal coefficient and R_{out} the output impedance of the latch system. The input referred noise for M5-M8 can be derived as,

$$V^2_{n,th,in}(T_{int}) = \frac{V^2_{n,th,out}(T_{int})}{A^2_{latch}} \tag{15}$$

where A_{latch} is the voltage gain of the latch. Henceforth, considering the operating state of each transistor in the evaluation phase, the latch gain can be given as,

$$A_{latch} = \left(g_{m5,6} + g_{m7,8}\right)R_{out} \tag{16}$$

substituting A_{latch} from Equation (16), Equation (15) leads to

$$V^2_{n,th,in}(T_{int}) = \frac{8kT\gamma}{g_{m5,6} + g_{m7,8}} \tag{17}$$

By adding those two components, the total input referred noise of the designed comparator is given as:

$$E^2_{n,th,in},(T_{int}) = \frac{2nkT}{C_L.\Delta V_{Fi,cm}(T_{int}).\left(\frac{g_{m16,17}}{I_{cm}}\right)_{T_{int}}} + \frac{8kT\gamma}{g_{m5,6} + g_{m7,8}} \tag{18}$$

As highlighted in Equation (18), it is evident that a large $\left(\frac{g_{m16,17}}{I_{cm}}\right)$ combined with a large $g_{m5,6}$ & $g_{m7,8}$, is needed for improving the noise performance of our proposed design. To get the lowest possible noise at a given current, it is desirable to maximize $\left(\frac{g_m}{I_{cm}}\right)$ for the differential input, which means that it is desirable to let M16 and M17 operate in weak inversion until the latch stage makes decision [30]. It can be concluded that by using the auxiliary devices sized to keep their transconductance sufficiently high and increasing $\left(\frac{g_{m16,17}}{I_{cm}}\right)$ for the differential input amplifier, the thermal noise of the proposed dynamic latch comparator is reduced.

3.6 | Time delay of the proposed DLC

The total delay time in this design is the addition of two components; the delay of the load capacitive discharge (t_{dis}) which is the period from the rising edge of the clock to the time when Outp and Outm are charged to V_{THN}; and the delay of the latch due to the regeneration (t_{latch}).

$$t_{delay} = t_{dis} + t_{latch} \tag{19}$$

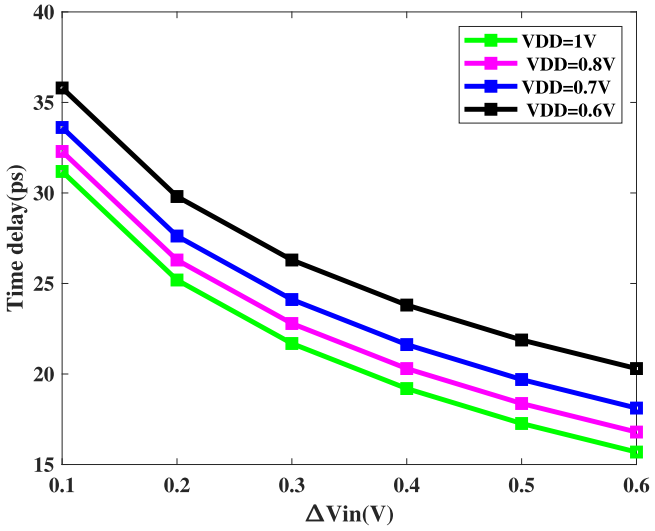

FIGURE 9 Delay of the proposed comparator versus differential input voltage (V_{DD} = 1 V, V_{cm} = 0.5 V, Clk = 20 GHz)

$$t_{dis} = \frac{V_{THN} C_{out}}{I_P} = \frac{2V_{THN} C_{out} \mu_p C_{ox} \frac{W_P}{L_p}}{g_{m,eff}^2} \tag{20}$$

$$g_{m,eff} = g_{mP} + g_{mN} = g_{mP}\left(1 + \frac{g_{mN}}{g_{mP}}\right) \tag{21}$$

$$g_{mP} = \mu_P C_{ox} \frac{W_P}{L_P} (|V_{GSP}| - V_{THP}) \tag{22}$$

$$g_{mN} = \mu_N C_{ox} \frac{W_N}{L_N} (V_{GSN} - V_{THN}) \tag{23}$$

Therefore, t_{dis} can be derived as follow:

$$t_{dis} = \frac{2V_{THN} C_{out} \mu_p C_{ox} \frac{W_P}{L_p}}{g_{mP}^2 \left(1 + \frac{g_{mN}}{g_{mP}}\right)^2} = \frac{t_0}{\left(1 + \frac{g_{mN}}{g_{mP}}\right)^2} \tag{24}$$

where t_0 is the period from the rising edge of the clock to the time when Outp and Outm are charged to V_{THN} considered in the conventional DLC [14]. However, the delay of the latch is given by equation.

$$t_{latch} = \frac{C_{out}}{g_{m,eff} + g_{m11,12}} \ln\left(\frac{\frac{V_{DD}}{2}}{\Delta V_0}\right) \tag{25}$$

$g_{m,\text{eff}}$, being the effective trans-conductance of the back-to-back inverter, and ΔV_0 the difference of the initial output voltage of the latch at the beginning of the regeneration process.

$$\Delta V_0 = g_{m16,17}(g_{m5,6} + g_{m7,8}) \frac{\Delta V_{in}}{C_{out}} t_{dis} \tag{26}$$

Equations (25) and (26) lead to the following formula of the total time delay.

$$t_{delay} = \frac{t_0}{\left(1 + \frac{g_{mN}}{g_{mP}}\right)^2} + \frac{C_{out}}{g_{m,eff} + g_{m11,12}} \ln\left(\frac{\frac{V_{DD}\left(1 + \frac{g_{mN}}{g_{mP}}\right)^2}{2}}{g_{m16,17}(g_{m5,6} + g_{m7,8}) \frac{\Delta V_{in}}{C_{out}} t_0}\right) \tag{27}$$

Further computations of Equation (27) lead to the developed expression given as;

$$t_{delay} = \frac{t_0}{\left(1 + \frac{g_{mN}}{g_{mP}}\right)^2} + \frac{t_{latch}}{1 + \frac{g_{m11,12}}{g_{meff}}} + \frac{2C_{out}}{g_{m,eff} + g_{m11,12}} \ln\left(\frac{1 + \frac{g_{mN}}{g_{mP}}}{g_{m16,17}(g_{m5,6} + g_{m7,8})}\right) \tag{28}$$

where, t_0 and t_{latch} are the delay of the pre-charge and the evaluation phases respectively in the CDTC and in the comparator in Ref. [14]. In this equation, the third term has a negative contribution since, M5-8, M16 and M17 are designed so that, $g_{m16,17}(g_{m5,6} + g_{m7,8}) > \left(1 + \frac{g_{mN}}{g_{mP}}\right)$. Therefore, the total delay time is reduced at a great extent.

Equation (28) represents the effect of various parameters on the total delay time. As depicted in that equation, the time delay of the preamplifier in the proposed structure is a fraction of the corresponding delay for the conventional structure. For a better optimization of time delay, furthers analysis should be carried on depending on the correlation between time delay and each of those parameters [14].

4 | SIMULATION OUTCOMES AND DISCUSSION

4.1 | Simulation and implementation framework

To achieve high-performance behaviour, our comparator is optimized with custom transistor sizing during the design process. The performances of the proposed circuit were verified using LTSpice simulator and the layout was implemented in 65 nm CMOS technology process from TSMC, using Electric VLSI. For general simulation purpose, the supply voltage was V_{DD} = 1 V, the common-mode voltage V_{cm} = 0.6 V, the differential input voltage level ΔV_{in} = 10 mV, the frequency of the clock signal was set to 20 GHz and the frequency of the input signal to 4 GHz. The load capacitance C_L and the output one C_{out} was set as 3.8 fF during the simulations. Monte-Carlo

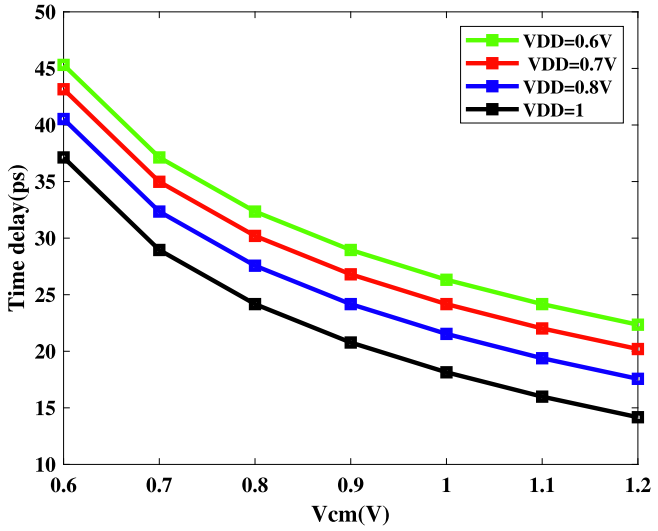

FIGURE 10 Delay of the proposed comparator versus input common mode voltage (V_{DD} = 1 V, ΔV_{in} = 0.5 V, Clk = 20 GHz)

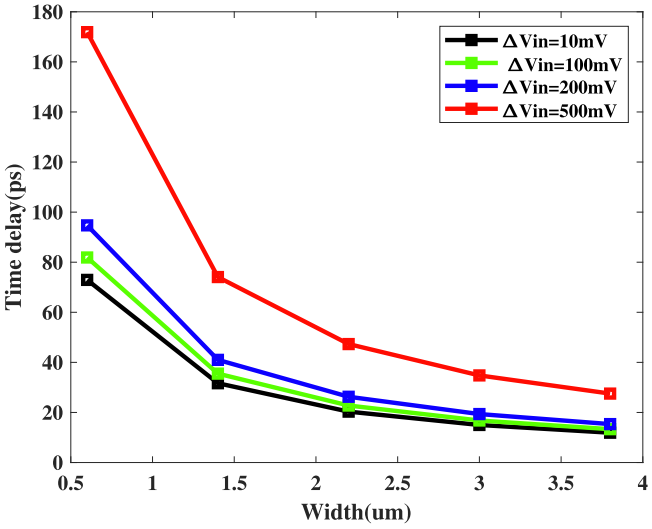

FIGURE 11 Delay of the proposed comparator versus the width of switches M5 and M6

simulation was performed for 500 runs and the histograms of the offset voltage and time delay were extracted.

4.2 | Result and discussion

The design parameters of the proposed comparator were improved as compared to CDTC and comparators which have been proposed in Ref. [21] and refs [1,15,18]. Figure 8 demonstrates the dependency of the proposed comparator delay on various differential input voltages level at different supply voltages. For a given V_{DD} = 1 V, the delay is 35.6 ps at differential input voltage level $\Delta V_{in} = 10\ mV$. This delay falls from 35.6 to 14.8 ps while ΔV_{in} varies from 10 to 500 mV. Furthermore, at a particular ΔV_{in}, the higher the supply voltage (V_{DD}), the higher the comparator delay will be. The worst-case delay of 35.6 ps for V_{DD} = 1 V for ΔV_{in} = 10 mV and the best of 14.8 ps for V_{DD} = 0.8 V and ΔV_{in} = 500 mV; the common-mode voltage being set to 500 mV (0.5V_{DD}). The effect of the input common-mode voltage (V_{cm}) on the delay of the comparator was simulated for 500 mV differential input under different supply voltages, and the results are shown in Figure 9. When V_{DD} = 1 V and V_{cm} = 500 mV, the delay is found to be 47 ps. For a fixed value of V_{DD}, the delay decreases while the input common-mode voltage (V_{cm}) increases. As illustrated in Figure 9, the delay is sensitive to the input common-mode voltage. The worst-case delay of 47 ps is exhibited for $V_{cm} = V_{DD}$ = 0.5 V and the best case of 14.4 ps was controlled for $V_{cm} = V_{DD}$ = 1 V.

Figure 10 shows the simulated delay of the proposed comparator with different widths of switches M5,6. As illustrated in Figure 10, when the width of those switches is larger than 3 µm, increasing the width would not help to reduce significantly the delay. For instance, at a given ΔV_{in} = 10 mV, the delay drops from 77 to 13.8 ps, as width drops from 0.6 to 4 µm. The delay becomes almost constant

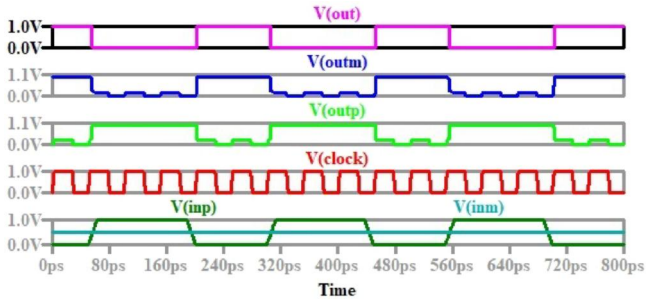

FIGURE 12 Post layout simulation of the time response of the proposed dynamic latch comparator (V_{DD} = 1 V, V_{cm} = 0.5 V, ΔV_{in} = 0.5 V, Clk = 20 GHz, C_{out} = 3.8fF)

for widths larger than 3.2 µm. In these considerations, the extracted value of the delay is found to be 13.8 ps.

The proposed dynamic comparator was simulated using 65 nm TSCM technology. The lengths of NMOS and PMOS are taken as 65 nm except M5 and M6 which lengths are 0.13 µm. The widths are sized to guarantee low offset, optimal time delay and small die area by reducing the $\frac{W}{L}$ ratio. For instance, as depicted in Figure 9, the widths of switches M5 and M6 are found to be 3.2 µm, for and optimal time delay of 12.15 ps. The clock frequency was set to 20 GHz and the input signal frequency to 4 GHz. The voltage supply was 1 V with common-mode input voltage of 0.5 V and 100 mV ΔV_{in}. The post-layout simulation of the proposed comparator is illustrated in Figure 11, with 3.8fF as extracted load capacitor at the Outm and Outp nodes of the latch. It is observed from Figure 11 that, with 1 V positive step for the input V_{inp} and keeping V_{inm} fixed to 0.5 V, V_{cm} = 0.5 V and Clk = 20 GHz the proposed dynamic latch comparator can switch successfully. V_{outp} and V_{outm} are the latch's output voltages and V_{out} stands for the comparator's output voltage after filtering noise

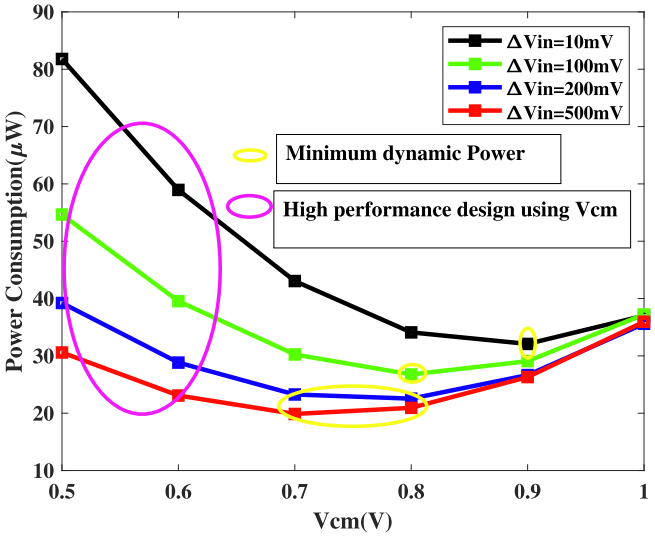

FIGURE 13 Simulation results of the power consumption versus input common-mode voltage, at various ΔV_{in} (Clk = 20 GHz and V_{DD} = 1 V)

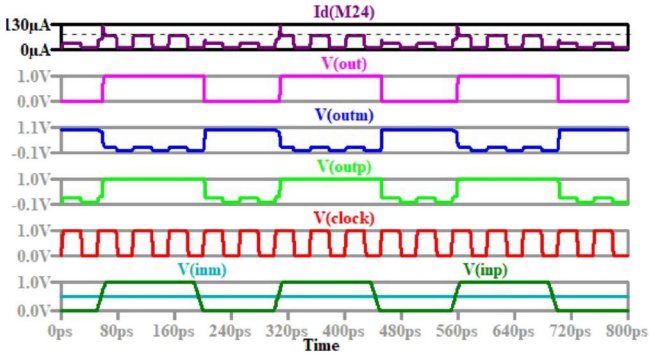

FIGURE 14 Post-layout simulation results for the average current of the proposed dynamic latch comparator

coming from the latch. In fact, the last stage of the circuit, which is a buffer as shown in Figure 12, plays an important role in filtering the noise coming from the latch. Due to the hysteresis present in the output buffer, the output transition will take place only when the latch output is sufficiently high or low resulting in sharp, well-defined digital data [24,28,30]. Definitely, V_{out} is immune to noise and the delay can be evaluated easily.

The effect of the common-mode voltage, V_{cm}, on power dissipation at various ΔV_{in} is simulated and the results are presented in Figure 13. It can be seen that power dissipation decreases with increase in V_{cm} from 0.5 to 0.9 V, at particular ΔV_{in}. However, for V_{cm} swing from 0.9 to 1 V, power dissipation increases but remains lower when compared to previous amplitude. For $\Delta V_{in} = 10\ mV$, the power dissipation is reduced from 81 μW at V_{cm} = 0.5 V to 38 μW at V_{cm} = 1 V. In general as depicted in Figure 13, the proposed comparator has less dependency on the V_{cm} due to the absence of the static power dissipation. The impact of transistor

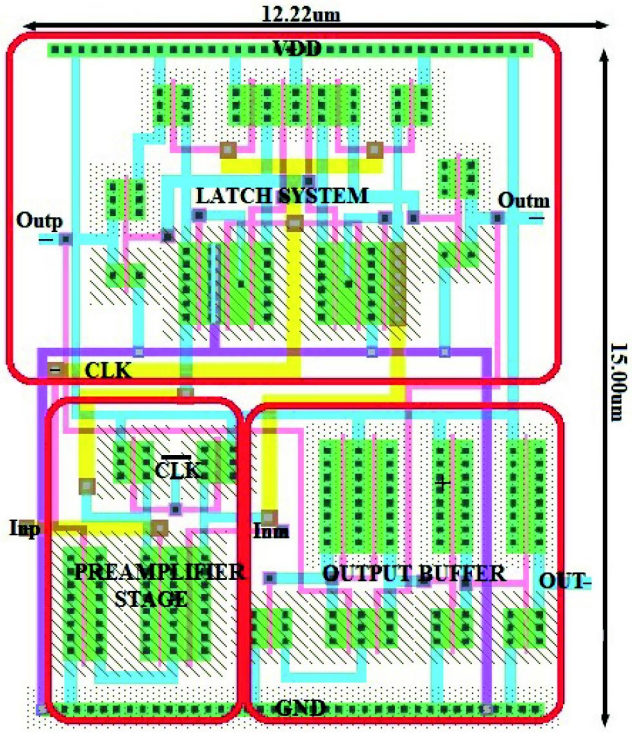

FIGURE 15 Layout diagram of proposed dynamic latch comparator using TSMC 65 nm CMOS technology

mismatch was evaluated while performing Monte-Carlo simulation.

Our design consumes very low amount of current exhibited in Figure 14. The post-layout simulation results show that the comparator circuitry requires only 67.8 μA, which is an average current for 20 GHz clock frequency. Moreover, the power dissipation of the design is 67.8 μW under 1 V voltage supply. The factor that significantly embodies the speed of a dynamic comparator is the propagation delay [22]. Generally, that parameter is inversely proportional to the input voltage applied. Moreover, a larger input voltage applied will increase the propagation delay [10,24,30]. The maximum operating frequency of the latch circuit is set by the propagation delay. In this work, the average propagation delay was extracted taking into account robustness of the design against process variation through a statistical analysis.

The circuit core layout is presented in Figure 15 where the chip occupies a small die area of 183.3 μm2. The mismatch and parasitic capacitance were reduced during the design process, using a parallel arrangement of all the transistors of the circuits. The post-layout Monte-Carlo simulation results for the offset voltage and time delay was performed to verify the reliability and the robustness of the design as depicted in Figure 16a,b) for 500 runs, respectively when ΔV_{in} = 0.5 V, V_{cm} = 0.5 V and the clock frequency being set to 20 GHz while using 1 V supply voltage. As shown on those plots, the average offset voltage of the circuit was controlled at 4.45 mV, while the standard deviation was 3.74 mV. Moreover, the average delay of the proposed design was only 14.28 ps while the delay

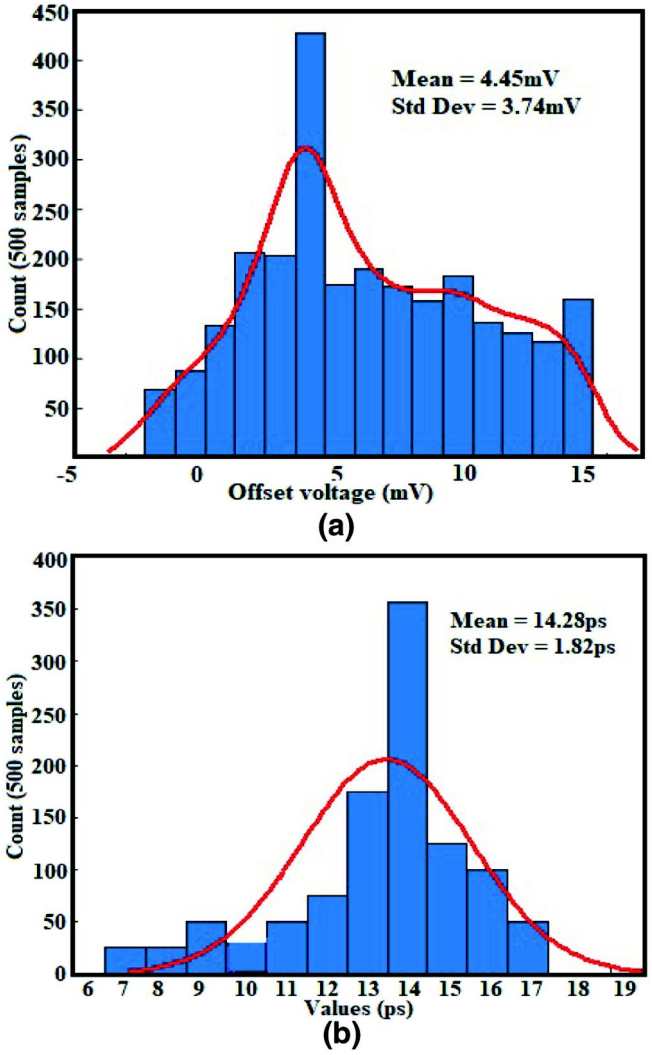

FIGURE 16 Monte Carlo results of both the offset voltage (a) and time delay of the proposed dynamic latch comparator (b) for 500 runs (V_{DD} = 1 V, V_{cm} = 0.5 V, ΔV_{in} = 0.5 V, Clk = 20 GHz, C_{out} = 3.8 fF)

standard deviation was controlled at 1.82 ps. By the way, the effects of the internal capacitances of the MOS devices is taking into account through the extracted parasitics. That affects the output voltage of the latch circuit, involving kickback noise rather than affecting the speed of the device. The achieving delay makes the clock of the latch signal faster up to 20 GHz, and achieves therefore a low-power behaviour with high-speed operations. Furthermore, the delay due to the amplification (regeneration phase) achieved in this design, is about 8 ps which represents 0.67 t_0; t_0 being the delay during the reset phase in Ref. [21]. So, adopting the auxiliary transistors help in lowering up to 33% the time delay of the amplification phase proposed in Ref. [21].

Corner analysis was performed via PVT variations for several different process corners (FF, FS, SF and SS) and temperatures, to demonstrate the global variation of the power consumption as depicted in Figure 17. Mismatch being a function of threshold voltage (V_{TH}) and supply voltage (V_{DD}), low V_{TH} (LVT) transistors have a reduced mismatch impact

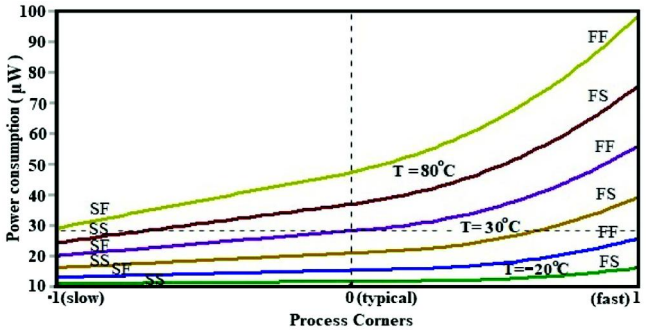

FIGURE 17 Simulation showing power consumption versus process variations and temperature

due to higher $\frac{V_{DD}}{V_{TH}}$ ratio than standard V_{TH} (SVT) or high V_{TH} (HVT) transistors [20,26]. The proportionate change in temperature from SVT to HVT is much larger as compared to that from LVT to SVT. Thus, it is more advantageous to move from HVT transistors to SVT devices, but this result in high power dissipation with the different corner process (FF and FS) for temperature of 80°C [26]. Although the increase in HVT can reduce percentage mismatch and power dissipation at temperature (−20°C and 30°C) for FF and FS corners. Large MOS devices increase the intrinsic parasitic which leads to more kickback noise and offset, but also reduce local head transfer and mismatch for LVT [26]. Taking into account trade-off between transistor size and mismatch, the optimal design technique (transistors sizing/matching) consisted of parallel arrangement of the devices to reduce the parasitic and mismatch effects, cancelling therefore the short circuit power generated by those parasitics. Difference in the NMOS and the PMOS characteristics can create short-circuit power consumption [25,26]. Moreover, local mismatch effects on transistors can exacerbate the situation. The effect is relatively small compared to switching and leakage power. It can be shown on Figure 17 that SS and SF corners at different temperatures (−20°C, 30°C and 80°C) were prone to ultra-low power dissipation design, but would slow down the changing rate of the transistors. A such of condition would have significant effect on the input transistors (M16 and M17) of the preamplifier and the pull-up transistors (M9 and M10) of the latch, thus producing low-speed operations.

In Table 1, the comparison of the proposed circuit for special overall performance parameters is illustrated with some preceding existing topologies. Using 65 nm CMOS technology process, the circuit exhibited lowest power delay product (PDP) of 0.968 fJ at 1 V supply voltage with 20 GHz clock frequency. The smallest time delay, PDP and highest clock frequency were achieved for the purpose. Then, exhibited a higher speed with a satisfactory amount of power consumption and die area.

The comparator in Ref. [1] has a lower offset voltage and die area from simulation result, but its power consumption is more than 4x higher than that of our proposed comparator. The comparators in Ref. [15] and Ref. [18] have lower power dissipation but suffer both from lower speed and larger offset

TABLE 1 Performance comparison of the proposed dynamic latch circuit with previous works

Comparison properties	[18][a]	[14][b]	[21][a]	[17][a]	[1][a]	[15][a]	[This work][a]
Technology (nm)	90	180	180	45	65	90	65
Supply voltage (V)	1	1.2	1.8	0.8	1.2	1	1
Clock frequency (GHz)	1	0.5	0.5	14.7	6	1	20
Delay time (ps)	51.76	268.6	638.91	268	42.7	148.23	14.28
Power consumption (μW)	32.62	72.2	347	5.8	381	14.46	67.8
Offset voltage (mV)	7.7	7.3	7.78	3.16	3.87	1.35	4.45
PDP (fJ)	1.67	19.4	221.7	1.55	16.3	2.144	0.968
FOM (fJ/Conv)	32.62	112.5	694	63.5	63.5	1.35	3.39
Die area (μm2)	58.32	252	361	26.92	141.7	74.32	183.3

[a]Simulation.
[b]Measurement.

voltage. The proposed topology achieves the maximum clock frequency of 20 GHz. As results, this comparator can be used to boost the performances of high-speed ADCs. The inconvenience of the NMOS transistor's source driving $V_{DD}-V_{THN}$ when its gate and drain are biased by V_{DD} is used in the load transistors of the differential amplifier, as an advantage in reducing the output nodes swing of the preamplifier and then lowering the power dissipation of the proposed comparator up to 42% of the power dissipation of the conventional comparator and 6% comparing to Ref. [21]. A figure of merit (FOM) must be agreed upon for comparison with previous research works. The following FOM was defined to highlight the performances of this design with recently published work Ref. [32].

$$FOM = \frac{P_d}{F_s}(J/Conversion) \tag{29}$$

where, P_d is the power dissipation and F_s being the comparator's sampling frequency. From Table 1, the proposed DLC exhibited a quite low and satisfactory FOM.

5 | CONCLUSION

The problems and shortcomings of the conventional double tail comparator have been analysed in terms of time delay and offset voltage. The topology was customized to improve the regeneration speed and power dissipation of the circuit. New dynamic latch comparator architecture is therefore proposed. The design uses a differential pair based NMOS enhancement active load as preamplifier stage; this reduces the power dissipation and increases the comparison speed. Short circuit current was reduced in the latch stage thanks to auxiliary transistors which isolated the latch module to the ground state. The parasitic and mismatch were reduced adopting custom design and transistors matching/sizing during the design process. A compact architecture was therefore obtained and the regeneration process was speeded up. Thus, offset and kickback noise were reduced and the time delay was improved. Simulations were carried out in 65 nm CMOS technology and the results confirm that the parameters are improved to a great extent. Analytical results were validated by post-layout simulation results. The post layout Monte-Carlo simulation outcomes clearly reveal that the circuit achieves a maximum operating speed of 20 GS/s, with an average offset voltage of 4.45 mV and 3.74 mV standard deviation while propagating with 14.28 ps delay time with 1.82 ps standard deviation. Furthermore, the proposed comparator exhibited lowest PDP of 0.968 fJ and dissipates only 67.8 μW of power from 1 V supply. The percentage improvement in power consumption for the designed comparator is 42% and 6% as compared to the CDTC and comparator of Ref. [21] respectively. Moreover, chip layout of the proposed design occupies only 183.3 μm2 active die area. The achieved results are better than recently published researches and make the proposed comparator very suitable for accurate and high-speed ADCs.

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A 0.35μm Low-Noise Stable Charge Sensitive Amplifier for Silicon Detectors Applications

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Abstract: The Charge Sensitive Amplifier (CSA) is the key module of the front-end electronics of various types of Silicon detectors and most radiation detection systems. High gain, stability, and low input noise are the major concerns of a typical CSA circuit in order to achieve amplified susceptible input charge (current) for further processing. To design such a low-noise, stable, and low power dissipation solution, a CSA is required to be realized in a complementary metal-oxide-semiconductor (CMOS) technology with a compact design. This research reports a low-noise highly stabile CSA design for Silicon detectors applications, which has been designed and validated in TSMC 0.35 um CMOS process. In a typical CSA design, the detector capacitance and the input transistor's width are the dominant parameters for achieving low noise performance. Therefore, the Equivalent Noise Charge (ENC) with respect to those parameters has been optimized, for a range of detector capacitance from 0.2 pF – 2 pF. However, the parallel noise of the feedback was removed by adopting a voltage-controlled NMOS resistor, which in turn helped to achieve high stability of the circuit. The simulation results provided a baseline gain of 9.92 mV/fC and show that ENC was found to be 42.5 e–with 3.72 e–/pF noise slope. The Corner frequency exhibited by the CSA is 1.023 GHz and the output magnitude was controlled at -56.8 dB; it dissipates 0.23 mW with a single voltage supply of 3.3 V with an active die area of 0.0049 mm^2.

Keywords: CMOS; CSA; Front-End; Low- noise; Silicon detector

Nizkošumen stabilen ojačevalnik za silicijeve detektorje

Izvleček: Na naboj občutljiv ojačevalnik (Charge Sensitive Amplifier - CSA) je osnovni del vhodne elektronike različnih silicijevih senzorjev in večine sistemov detekcije sevanja. Veliko ojačenje, stabilnost in nizek šum so glavne zahteve tipičnih CSA vezij za doseganje zadovoljivega ojačenja naboja (toka) za nadaljnje procesiranje. Za razvoj nizko šumne, stabilne rešitve z nizko porabo mora biti CSA realiziran v kompaktni CMOS tehnologiji. V delu predstavljamo nizko šumen, stabilen CSA za silicijev detektor, ki je bil preverjen v TSMC 0.35 um CMOS tehnologiji. V tipičnem CSA sta kapacitiven detektor in vhodna širina tranzistorja glavna parametra za doseganje nizkega šuma. Ekvivalenten šumni naboj ej bil optimiran za detektiranja kapacitivnosti v razponu od 0.2 pF – 2 pF. Paralelni šum povratne vezave je bil odstranjen z napetostno krmiljenim uporom, ki je pripomogel tudi k stabilnosti vezja. Simulacije so pokazale ojačenje 9.92 mV/fC in ENC 42. 5 e– z naklonom 3.72 e–/pF. Vogalna frekvenca CSA je 1.023 GHz, in kontroliranim izhodnim signalom pri -56.8 dB. Poraba moči je 0.23 mW pri 3.3 V napajanju in aktivni površini 0.0049 mm^2.

Ključne besede: CMOS; CSA; vhod; nizek šum; silicijev detektor

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1 Introduction

The Modern Front-End Electronics (FEE) for High Energy Physics Experiment (HEPE) are mixed-signal circuits in which the ultimate performance is set by the analog circuit applied to Solid State Detectors. The X-Rays-Sensors interaction produces a very small current and has to be amplified in a low noise circuit before any further signal processing either on-chip or off-chip with digital techniques. In multi-detector systems, multiple channels create several complications. In order to limit the power dissipation-noise problem, the sensor should be placed adjacent to the front-end amplifier. However, this results in decreased detector resolution because of heat transfer. Moreover, the process technology utilized for designing a preamplifier determines the overall size and price of the silicon-based detector systems. When a soft X-rays strikes a semiconductor detector, charges are generated. Various types of X-ray detectors including Silicon PIN Detectors, Silicon Drift Detectors (SDDs), Silicon Strip Detector (SSD), etc. have been extensively used in order to quantify the energy and photon count of incident X-rays. This type of detectors designed with a thick Si substrate is very useful for 2-D tracking in a high multiplicity environment because of the large charge collection area along with low anode capacitance [1]. Through going X-rays, create electron-hole pairs in the depletion zone of the detector and these charges drift towards the electrodes as illustrated in Fig.1. This drift (current) creates the signal (voltage) which is very weak and must be amplified by a CSA connected to each strip.

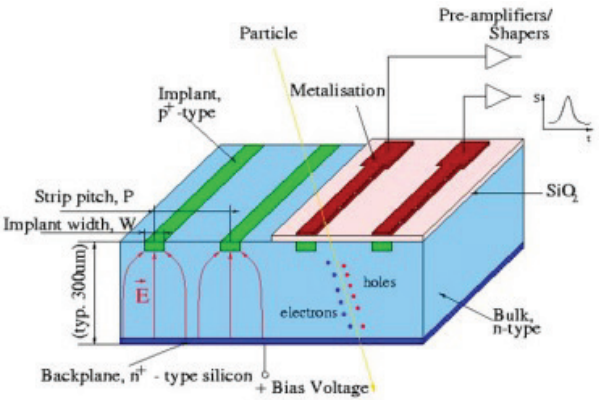

Figure 1: Principle of operation of a silicon strip detector [2].

From the signals on the individual CSA, the amplitude of the output voltage is realized. That voltage depends on the energy of the incident particles and must be measured with the highest accuracy and precision [3]. The input node voltage of the CSA increases and the voltage with the opposite polarity is generated at the output terminal simultaneously. Hence, the output potential through feedback loop forces the input potential of the CSA to become zero because of high open-loop gain as evident from Fig.2. The total amount of the current pulses is integrated on the feedback capacitor and the corresponding output is a step voltage pulse [3, 4] as described in equation (1).

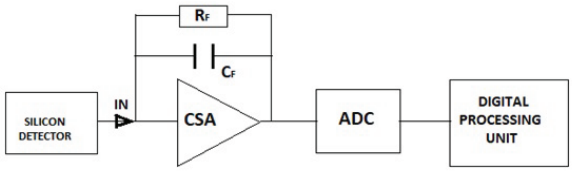

Figure 2: Silicon detector readout architecture for digital processing, the CSA is used for extracting the charge at each strip and convert it into voltage.

$$V_{CSA}(t) = \frac{1}{C_f}\int_0^T i_e(t)\,dt + V_0 \quad (1)$$

Where, VCSA(t) is the output voltage of the CSA at the time t, $i_e(t)$ is the input current injected in the detector, T is the integration period, C_f the feedback capacitor and V_0 is the offset voltage of the circuit.

As the input signals intercepted by CSA are generally very low. For a given signal source, the CSA noise performance depends on the noise created within the amplifier itself and the signal impedance seen by the amplifier input. Therefore, the CSA input stage must ensure that optimum noise matching is obtained for the given source impedance. The choice of the design parameters of the input stage of CSA influences the noise matching. So the total equivalent input noise should be kept as small as possible for a given detector capacitance up to 2pF. The main problem in the design of nuclear spectroscopy Very Large Scale Integration (VLSI) readout front ends is the implementation of low-noise; low power Charge Sensitive Amplifier (CSA). The selection of the process (CMOS or BiCMOS) determines the performance and generally the noise-related design methodology. A VLSI preamplifier costs much less than a hybrid one or a preamplifier unit [5]. CMOS exhibits several advantages over other concurrent technologies and and is preferred in VLSI circuit design [6-7]. A very popular approach in designing the VLSI CSA is the usage of an operational amplifier (Op-amp), with the R-C feedback network. Since Cdet (the detector parasitic capacitance) is quite large, about 15pF, the stability becomes a critical issue in that design [8]. For a complete validation of the CSA with CMOS technology, the overall system specifications are needed [8, 9]. In [10] H. Wang et al, proposed a CSA based Polyvinylidene Fluoride (PVDF) transducers. The circuit

works for low power dissipation and low frequency; but it iss prone to low conversion gain, high feedback capacitance that occupies more die area. A. Baschirotto et al [11], designed a CSA using a single-ended amplifier. The circuit works at high frequency and very low voltage; however, the disadvantages of that circuit are high power consumption and high Equivalent Noise Charge (ENC); furthermore, the circuit was prone to the parallel noise generated by the feedback resistor. The single-ended amplifier is a good architecture despite it is prone to both process variations and signal degradation. Indeed, the current mirrors, which generate the bias voltage for proper operation of the amplifier, contribute the common-mode noise. Thus, increasing the size of the input transistor of such an amplifier does not improve noise performance because of the bias current limitation [4]. Therefore, it is necessary to propose an optimal circuit to avoid unnecessary power dissipation and heat in closely packed pixel arrays. Secondly, the ENC should be optimized with respect to detector capacitance and the input transistor width, by performing AC and transient analysis.

In this article, a low-noise CSA designed in 0.35 µm CMOS technology process is proposed. The circuit consists of a single-ended gain block and a feedback network. The CSA bandwidth is compromised by a large detector capacitance. In order to compensate this, a common-source (CS) input design is adopted to isolate the capacitance, preventing it from affecting the bandwidth. Furthermore, CS topology is linear and power-efficient [12]. The feedback resistor stabilizes the gain-bandwidth product of the circuit. The resistor is an NMOS transistor operating as a voltage-controlled resistor; it also reduces the parallel noise contribution. The proposed circuit works with a low-energy capacitive silicon detector for X-ray detection applications.

2 Materials and methods

The CSA has been designed for a 0.35 µm TSMC process, to perform the initial conversion of current pulses into voltage pulses. Table 1 below presents the design specifications of a CSA circuit for Silicon-PIN detector applications.

Table 1: CSA specifications required for silicon detector for two vendors.

Vendor Parameters	Hamamatsu (H4083)	Amptek (A250)
Power consumption	150 mW@12V	14 mW@6 V
Count rate	2.6 MHz	2.5MHz
Detector capacitance	0 – 25 pF	0 – 250 pF
ENC (Cin = 5pF)	240 e-	76 e-
Noise slope	4 e-/pF	11.5 e-/pF
Sensitivity	22 mV/MeV (Si)	176 mV/MeV (Si)

In order to increase the gain of the CSA, we choose a three-stage configuration for the design. The single-ended configuration of the circuit in Fig. 3, is preferred to the differential one for the reduction of power consumption. The choice of the N-channel input transistor relies on the lower thermal noise compared to the P-type at high frequency, since the 1/f noise is negligible in the frequency region after 10 kHz [13, 14]; in addition, N-channel MOS, gives a lower series white noise with respect to the P-channel counterpart, because of its higher transconductance [13]. The current source at M1's drain is provided by M2, a P-channel MOSFET with smaller transconductance.

The second stage is the Miller stage. In this stage, the transistors M3 and M4 are connected in cascade whereas the transistor M5 forms the current mirror. Such a stage in the CSA incorporates a higher output resistance. The maximum signal swing must be kept limited so that all the transistors remain in the saturation region of operation, i.e., VGS> VT and VDS> VGS-VT [13]. Therefore, the bias current of M3 is kept at a specific low value (12.5 uA) in order to keep its output impedance high. Capacitor Cm provides a gain and the dominant pole in that stage; so, resistor Rm suppresses direct transmission through Cm at high frequencies.

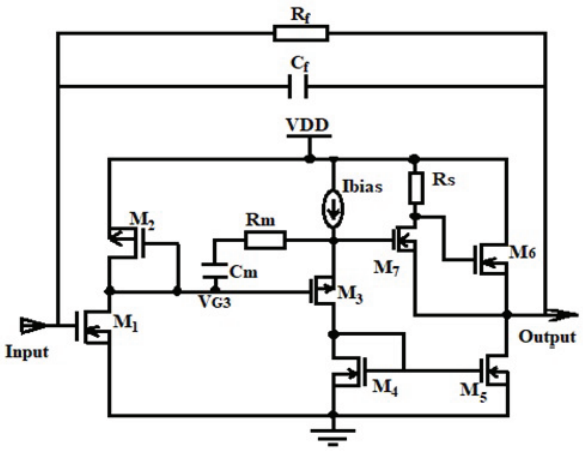

Figure 3: Schematic of the proposed structure of the CSA.

The third stage consists of an N-channel MOSFET M7 which results in a negative gain of the entire circuit so that one can apply the negative feedback. It is biased by a low current through RS. The value of Rs is set to

300 Ω so that M7 operates in the saturation region. Feedback from Vout is connected to one of the two inputs through an on-chip feedback capacitor up to 20 pF and a resistor of 30 MΩ at the top-level design. The circuit was designed with thick oxide transistors that allow a relatively high supply voltage of 3.3 V in a standard 0.35 µm CMOS technology process.

2.1 Analysis of the CSA circuit

The first stage is a cascade topology based on a common source amplifier so that the input is free from parasitic capacitance and the feedback amplifier controls the gate voltage. Therefore, the CSA input becomes a virtual ground and the detector capacitance is less significant to the CSA bandwidth.

The drains of M1 and M2 are common. When M1 is in the saturation region, we have the equation bellow:

$$V_{G3} = |V_{THP2}| + |(V_{in} - V_{THN1})| \sqrt{\frac{\mu_n}{\mu_p}\left(\frac{W_1}{L_1}\right)\left(\frac{L_2}{W_2}\right)} \quad (2)$$

When M1 enters in the triode region, the following equation (2) holds

$$\mu_n\left(\frac{W_1}{L_1}\right)\left[2\left(V_{in} - V_{THN1}\right)V_{G3} - {V_{G3}}^2\right] = \mu_p\left(\frac{W_2}{L_2}\right)\left(V_{G3} - V_{THP2}\right)^2 \quad (3)$$

with this topology, the dopants are not concentrated near the surface, so their effect is less than expected. Therefore, the voltage at the gates of M2 and M3 should depend on Rm and the reference current of M2.

In the second stage of CSA circuit, transistor M3 is in the saturation region and its drain-source current is defined by the formula:

$$I_x = \frac{1}{2} C_{ox}\mu_p\left(\frac{W_3}{L_3}\right)\left(V_{G3} - V_{THP3}\right)^2 \quad (4)$$

Transistor M3 remains in the saturation region until the device enters the triode region where

$$V_{G3} = V_{THP3} + \sqrt{\frac{2I_{bias} + 2V_{THP3}/R_m}{C_{ox}\mu_p\left(\frac{W_3}{L_3}\right)}} \quad (5)$$

As the whole circuit is designed to work in the saturation region, equations (2) and (5) involve:

$$I_{bias} = C_{ox}\mu_p\left(\frac{W_3}{L_3}\right)\left[V_{THP2} - V_{THP3} + \left|\left(V_{in} - V_{THN1}\right)\right|\sqrt{\frac{\mu_n}{\mu_p}\left(\frac{L_2}{W_2}\right)}\right]^2 - \frac{V_{THP3}}{R_m} \quad (6)$$

The biasing current helps to deplete a larger portion of the substrate and the p-well. That current depends on both the geometric and threshold voltage of transistors M1, M2 and M3. Those parameters are influenced by the mismatch of the circuit. At threshold voltage of the transistor, the instantaneous current flowing from source to drain gets a sudden boost and the additional gate voltage rise causes an exponential increase of the current. The threshold voltage of a transistor is not constant and depends on physical, electrical, and environmental factors. It has two parts: ΔV_{TH0} that is supposed to be persistent for a given technology, device, etc. [15] and ΔV_{TH} that depends on operational parameters. The V_{TH} can be expressed in the equation (6) as

$$V_{TH} = V_{TH0} + \Delta V_{TH} \quad (7)$$

Assuming V_{TH0} constant for each transistor and ΔV_{TH} identical for each type of transistor, the final expression of Ibias can be expressed as follows:

$$I_{bias} = C_{ox}\mu_n\left(\frac{W_1 \times W_3}{L_3 \times W_2}\right)\left(V_{GS1} - V_{THN0} - \Delta V_{THN0}\right)^2 - \frac{V_{THP0}}{R_m} - \frac{\Delta V_{THP}}{R_m} \quad (8)$$

Fluctuations in ΔVTH occur mainly because of temperature and voltage variations which initiate effects such as Drain Induced Barrier Lowering (DIBL), short channel effects, narrow width effect, back bias dependent threshold shift, hot carrier effect, etc. So, the biasing current as a function of the threshold voltage was computed for the limited amount of current for the circuit [15] [16].

2.1 Noise optimization of the CSA circuit

One of the primary objectives of a typical CSA design is the minimization of the ENC and this necessitates a precise input stage design. In general, the noise associated with the drain current of the input device is the vital part of the ultra-low-noise design, [17]. Past research on ENC noise minimization in the CSA focused on the geometric characteristics (W and L) or the transconductance (gm) of the input transistor. However, the leakage current is a crucial parameter of the detector which seriously affects the resolution and reliability of the detector. It is related to many factors, such as the quality of silicon, process flow, temperature, etc. which is difficult to accurately express by analytical formula. Gate-controlled diodes have been frequently used to characterize leakage current components and extract minority carrier lifetime [16] [24]. Some detailed leakage current analyses with gate-controlled diodes have been performed in regular thickness wafer for a radiation detector [16]. This research, presents the ENC as a function of the detector capacitor and the feedback for a fixed value of W and L, according to the adopted

CMOS process. The leakage current is 10nA. The different contributions are evaluated as follows:

The most prominent thermal noise contribution can be calculated as:

$$ENC_{th}^{\ 2} = 4K_B Tn\gamma\alpha_n \frac{\left(C_{\det} + C_f + C_g\right)^2}{g_m C_g} \frac{N_{th}}{\tau_p} \quad (9)$$

In which KB is the Boltzmann constant, T is the room temperature, η is the body factor, γ is the inversion factor, αn the excess noise factor, Nth is the shaper noise index for the thermal noise, τp is the peaking time, Cdet the detector capacitance, Cf the feedback capacitance, Cg the gate capacitance and gm the input MOSFET transconductance.

The flicker noise or the noise due to 1/f is expressed as:

$$ENC_f^{\ 2} = K_f \frac{\left(C_{\det} + C_f + C_g\right)^2}{C_g} N_f \quad (10)$$

Where Kf is the flicker noise coefficient and Nf the shaper noise index for flicker noise. Considering the fact that, $g_m = \sqrt{2\mu \frac{C_g I_D}{L^2}}$ with Cg = Cox WL [12], equations (9) and (10) are respectively written as:

$$ENC_{th}^{\ 2} = 4K_B Tn\gamma\alpha_n \frac{\left(C_{\det} + C_f + C_{ox}WL\right)^2 L}{\sqrt{2\mu I_D}\left(C_{ox}WL\right)^{\frac{3}{2}}} \frac{N_{th}}{\tau_p} \quad (11)$$

$$ENC_f^{\ 2} = K_f \frac{\left(C_{\det} + C_f + C_{ox}WL\right)^2}{C_{ox}WL} N_f \quad (12)$$

The white parallel noise contribution to the MOSFET gate current due to the detector leakage current, can be written as:

$$ENC_i^{\ 2} = 2qI_{leak} N_i \tau_p \quad (13)$$

Where, Ileak is the leakage current associated with shot noise, and Ni is the shaper noise index for the shot noise. This term doesn't depends on W and ID.

Different components of the ENC were optimized with respect W and ID first, and the with respect to Cg. A first-order (n = 1) shaper has been used. Therefore the thermal noise is optimal if

$$\frac{\partial ENC_{th}^2}{\partial W} = 0 \quad (14)$$

Equation (14) is satisfied. The solution of that equation (14) is Wth = ((Cdet + Cf)/3CoxL), where, Wth = 42 µm for Cdet=Cf = 0.2 pF. Similarly, the flicker noise is optimal when equation (15) is satisfied.

$$\frac{\partial ENC_f^2}{\partial W} = 0 \quad (15)$$

The solution of that equation (15) is: Wf= 3 Wth with (Wf=126 µm).

The ENC as a function of ID and W is computed for both the thermal and the flicker noise. In this study, the lowest width (Wth= 42 µm) has been considered for achieving a minimal thermal noise contribution. The flicker (1/f) noise of the drain current of the preamplifier is associated with the input transistor. This is because of the generation and recombination of carriers in the two depleted regions from impurity atoms and lattice defects [16]. The instability of the drain current (ID) is established by the variation of charge in the depletion region, which constitutes the channel width. Therefore, an optimal width involves an optimal drain current of 70µA. If the trapping and releasing of carriers were purely random, the noise spectrum would be uniform. The ENC of the whole CSA circuit is calculated by adding the contributions of thermal noise, flicker noise and the shot noise [14, 17, 18]. In order to make noise as small as possible, Kf is needs to be as small as possible. Its value depends on the adopted technology process as well. Therefore, the total ENC can be expressed as:

$$ENC_{total}^2 = ENC_{th}^{\ 2} + ENC_f^{\ 2} + ENC_i^{\ 2} \quad (16)$$

$$ENC_{total}^2 = 4K_f N_f (C_f + C_{\det}) + \\ + \frac{64}{3} K_B Tn\gamma\alpha_n \frac{N_{th}}{\tau_p} \frac{\sqrt{C_{\det} + C_f}}{\sqrt{6\mu_n I_D}} + 2qI_{leak} N_i \tau_p \quad (17)$$

Where, ENC_{th}, ENC_f and ENC_i are the thermal flicker and shot noise components respectively. Mostly, ENC_{th} is the dominant part of overall ENC noise. Equation (14) is computed and the ENC could be represented by the following expression.

$$ENC = 42.5e^- + 3.72e^- / pF \quad (18)$$

Input transistor capacitance, Cin, contributes to the total capacitance of the input of the preamplifier, Ctot, which affects the series white noise and the 1/f noise contribution to the total noise. If the width of the gate-channel is reduced, Cin as well as the transconductance (gm) decrease, which results in higher series white noise spectral density. In order for the transconduct-

ance to be as large as possible, a relatively large width transistor is preferred [15, 18]. Moreover, if the detector capacitance dominates over the transistor capacitance, a large Cin value results in a small noise increment. However, such a Cin can be balanced by matching it to the detector capacitance. Table 2 and Table 3 illustrate the constant parameters used for this design and the transistor sizing for the proposed CSA design.

Table 2: Main constant parameters.

Symbol	Quantity	Values
n	body factor	1.5
α_n	excess noise factor	0.93
γ	inversion factor	0.53
N_f	shaper noise index for flicker noise	3.69
N_{th}	shaper noise index the thermal noise	0.92
K_f	flicker noise coefficient	$8.5.10^{-25}C^2m^{-2}$
g_m	input transistor transconductance	614 µS

Table 3: Transistor parameters (W/L).

Transistors	W/L (µm)
M1	42/0.35
M2	0.84/0.35
M3	18/0.35
M4	18/0.35
M5	12/0.35
M6	12/0.35
M7	9/0.35

3 Results and discussions

The proposed CSA circuit performance was verified using LTspice simulator and the layout was implemented in 0.35 µm CMOS technology process from TSMC, using Electric VLSI, which is an open source tool for integrated circuit design. Fig. 4 shows the gain of the proposed CSA. It is controlled by the Ibias value for a feedback loop of Rf = 150 kΩ and Cf = 2 pF. Frequency domain analysis was performed from 1Hz to 10 GHz. The bias current is adjusted by changing the value of the external resistor allowing changing the transconductance as represented in equation (7). The gain (absolute value) varied from 40.6 dB to 53.8 dB. The highest bandwidth of the amplifier is achieved for 12.5µA bias current, and is equal to 1.023 GHz. The optimization of the bias current of the second stage is very important for stabilizing the gain-bandwidth product and maintaining signal integrity [19]. The capacitor of the detector was set to 1 pF and the parasitic capacitance of the input transistor is around 20 fF. So, total input capacitance was 1.02 pF.

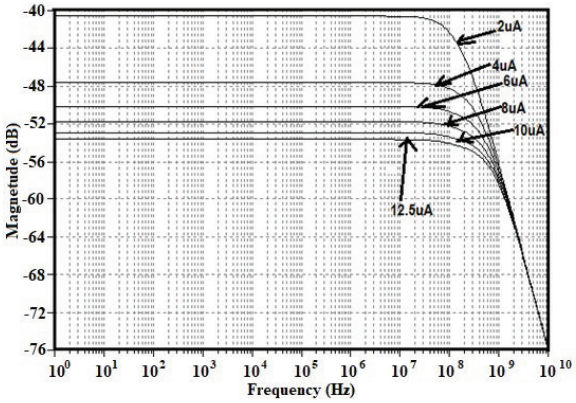

Figure 4: Influence of Ibias on the gain.

One of the most critical points in CSA is the loop gain stability, which is determined by its feedback capacitance. Nevertheless, a resistor has a parasitic capacitance and a capacitance has a parasitic resistance. Thus, an RC feedback network (Rf-Cf) models the feedback circuit. Loop-gain stability has been evaluated during the charge vs voltage conversion when Rf-Cf is bypassed [9]. The Opamp equivalent load capacitors are also taken into consideration by varying Cf. For achieving the highest stability of the circuit, the gain is adjusted by the Rf-Cf sizing. Rf was implemented by associating the drain-source resistance of a N-channel MOSFET device biased to be in the triode strong inversion region. Under this condition, the parallel noise was eliminated; the circuit is therefore stable and continuously sensitive and can be maintained in this condition without adjustment for spectroscopy purpose [10, 22, 23 and 24]. Thus, with that technique, we achieved a feedback resistance of 30 MΩ with a W/L = 25. The magnitude of the gain is therefore represented for each parameter of the feedback network. Thus, for Rf = 150 kΩ, Cf is varied from 2 pF to 20 pF. Fig.5 shows the variations of the gain for different values of Cf. For frequencies lower than 100 kHz, the parasitic capacitance of the input transistor and the resistive feedback affect the gain of the CSA and its bandwidth. The closed loop bandwidth achieved in this topology is 459.6 MHz. The circuit is immune to those parasitic effects for frequencies greater than 100 kHz. The same analysis could be applied to Fig. 6, where a MOSFET controller resistor, sized to be 150 kΩ, substituted the resistive feedback. The gain is immune to the resistive feedback and the parasitic capacitance. These results confirm the stability of the circuit with a feedback MOSFET resistor. A bandwidth of 1.023 GHz can be achieved without compromising the stability of the circuit (with output magnitude of -56.8 dB). By adjusting Ibias as shown in

Fig. 4, the bandwidth could be increased to more than 1.9 GHz.

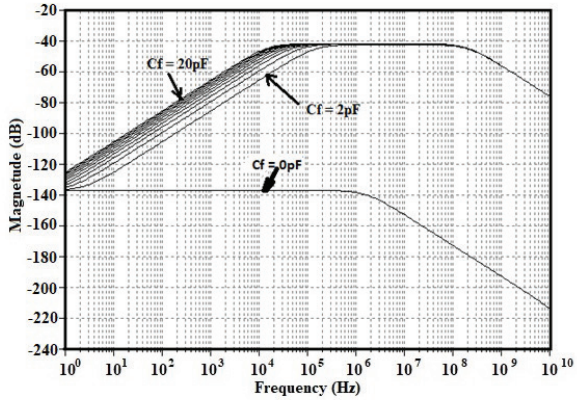

Figure 5: Influence of Cf on the gain with Rf feedback.

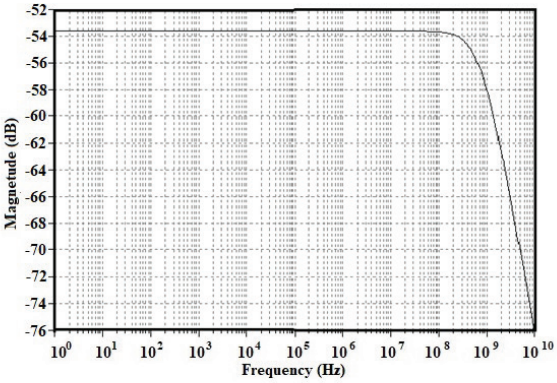

Figure 6: Influence of Cf on the gain using a MOSFET equivalent of Rf.

In Fig. 7 the Input-referred-noise (IRN) is plotted in the frequency range of 1 GHz to 10 GHz. The IRN (noise density) value extracted is 2.38 nV/√Hz. Furthermore, while designing a recording analog front-end (AFE), a lower IRN ensures the better signal quality and low power consumption will extend the lifetime of the device [19]. However, in the CSA, the parameter that embodies the noise performance is the ENC (Equivalent-Noise-Charge), namely the input charge necessary to get at the output a signal equal to noise. Its calculus was based on this intrinsic definition, neglecting the standard calculus depending on the post-CSA circuit, not present in this design [10]. Therefore, the ENC was computed and extracted based on equation (14); it presents a constant value of 42.5 e- for a detector capacitance of 0pF and noise performance increases with a slope of 3.72 e-/pF. For exhibiting the dominant component of the input noise, the ENC as a function of ID and W for the thermal component is computed in Fig. 8, and compared to the flicker noise component, which depends on W as shown in Fig. 8 and Fig. 9. In Fig. 8, when increasing the current in the input transistor, its thermal noise decreases but the bandwidth over which the thermal noise is integrated increases by the same amount; both effects cancel each other out. It can be depicted in Fig.8 and Fig .9 that the most dominant component of the ENC noise is the thermal noise component. Thus, if the device operates in a low count rate environment, substantial reductions in power consumption can be obtained with little or no noise penalty by reducing the bias current of the input transistor provided a good separation between the preamplifier rise and fall time is ensured [25].

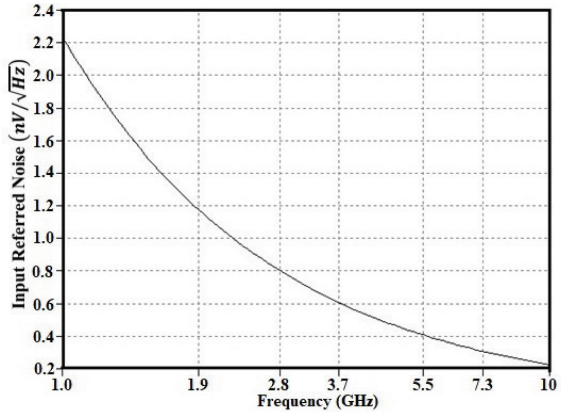

Figure 7: CSA Input-Referred Noise.

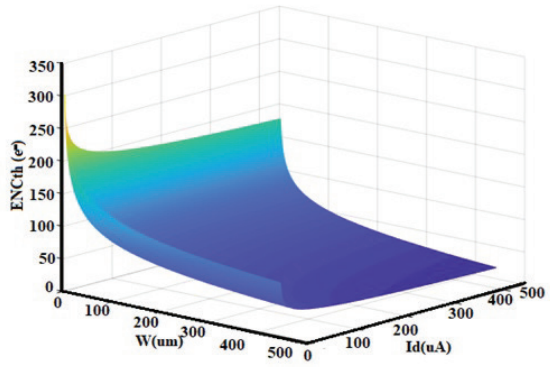

Figure 8: ENCth as a function of W and Id.

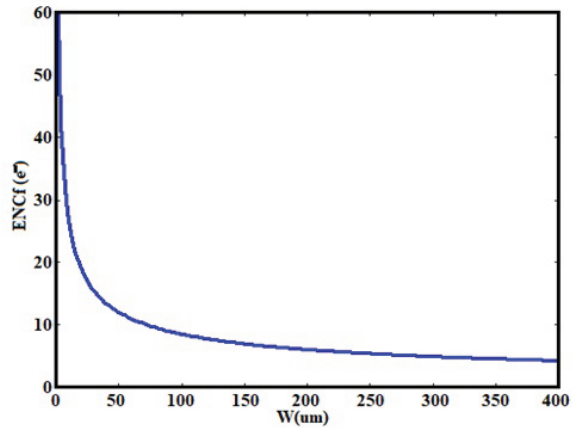

Figure 9: ENCf as a function of W.

The transient response of CSA is shown in Fig.10 and Fig.11. A current pulse with an amplitude of 33 µA and width of 1ns (206250 electrons) is injected into the detector. The output of CSA achieves a peak of 330mV and decreases thereafter because of the feedback action. For a detector capacitor of 0.2 pF, the bias current of M3 is varied and the results are shown in Fig.10. It is evident that Ibias helps to keep a lower offset and better resolution of the circuit. The same analysis is made by fixing the bias current at 12.5 µA and varying the detector capacitor from 0.2 pF to 2 pF on Fig.11. The highest amplitude (1.23 V) is obtained with 0.2 pF detector capacitance; while the highest capacitor (2 pF) generates saturation of the CSA. The output voltage is distorted and the energy information is lost which results in a circuit with low resolution. [5][26]. The fall time of the signal is about 300ns (determined by Cf and Rf).

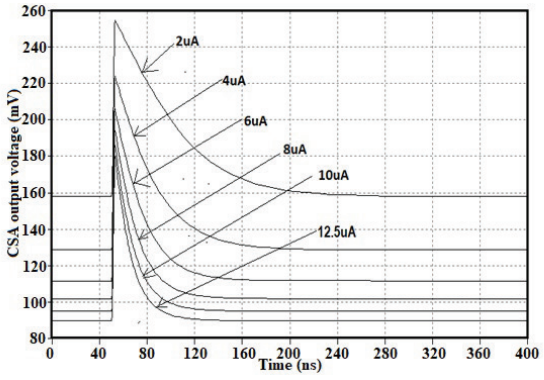

Figure 10: Ibias effect on CSA output voltage.

The amplitude of the signal charge obtained with a semiconductor detector is determined by the input particle energy such as soft X-rays and gamma rays and by the material of the semiconductor [14]. For Si-PIN diodes, the capacitance scales with area, so large area detectors exhibit more noise [21]. For SDDs, the capacitance is much lower and nearly independent of area. This noise is weakly dependent on temperature and leakage current. Since leakage current increases exponentially with temperature, reducing temperature helps dramatically [1].

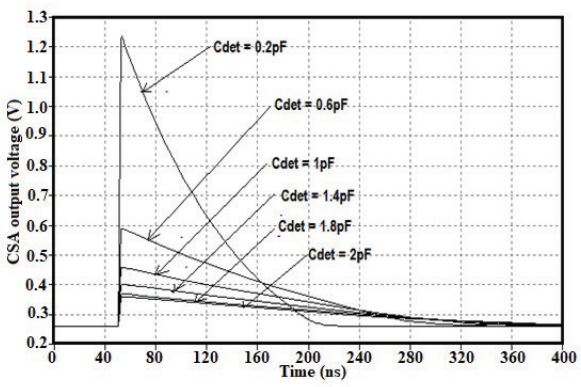

Figure 11: Cdet effect on CSA output voltage.

The total core layout area occupied by the proposed CSA is (88x55.7) µm2 as shown in Fig. 12. Parasitic extraction was used to extract the netlist with parasitic. The voltage supply is 3.3 V; the total power consumption is about 0.23 mW for the whole circuit. In this research, the gain-bandwidth product of the circuit was stabilized by means of a high-frequency feedback loop, which operates according to the voltage controlled NMOS resistor (Rf) technique [10] with resistance between 30 kΩ and 30 MΩ and a capacitance of 2 pF. The response of the circuit to different input charges results in good amplification. The gain linearity of the specific preamplifier implementation was extracted and the circuit energy response is shown on Fig. 13. The non-linearity of the CSA's gain shown on Fig. 14 (within 4.6% up to Qin=420 fC, and within 0.8% up to 300 fC) is mostly due to the second order effect of the dependence of Rf (MOSFET) on the input charge. The single MOSFET feedback network provides minimum thermal noise and high linearity, but requires baseline stabilization, and can be realized in multiple stages. [22]. The absolute value of the conversion gain is 9.92mV/fC.

Fig. 15 shows the Monte-Carlo results of the proposed circuit for 500 runs. The output signal and the histogram of the conversion gain of the circuit are shown for 10 fC injected at the input of the detector. The output signal varies from 100mV to 50 mV due to the variations of the different parameters of the circuits with the tolerance of 10%. In fact, the process variation of Ibias increases the dc-gain of the core amplifier as explained in the previous sections. The highest sensitivity of the design is then presented on Fig.15a, for a weak amount of injected charge (10fC); the circuit achieved an amplitude of 100mV. However, the histogram of conversion gain observed on Fig.15b shows a mean value of 9.79 mV/fC, and a standard deviation of 1.64 mV/fC. This indicates that the results obtained with Monte-Carlo models do not differ significantly for 500 runs and the CSA performance is quite stable and reliable.

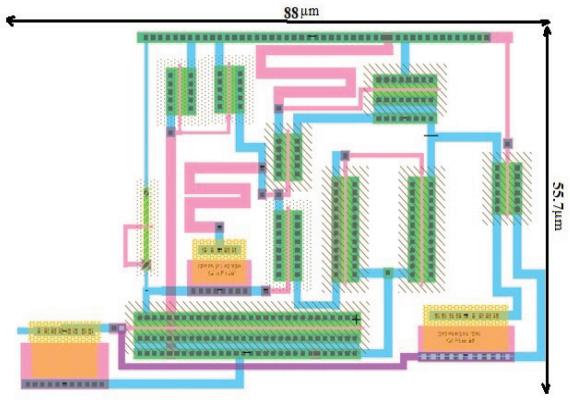

Figure 12: The core layout of the CSA circuit.

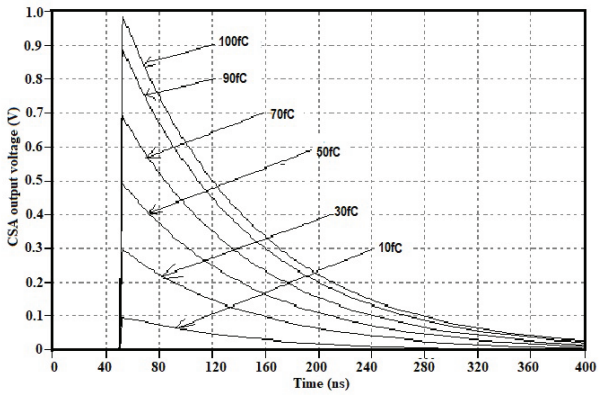

Figure 13: CSA output voltage for different input charge

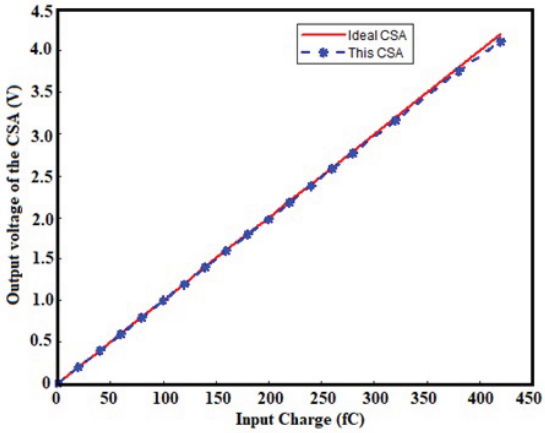

Figure 14: Output voltage vs input charge of the CSA circuit

As a summary, in Table 4 the overall features of the CSA circuit are shown. The effort in reducing power consumption, ENC and active die area of the chip comes in the parallel with similar application design present in literature [5, 8, 10, 11, 14, 21, 26]. Considering the significant difference in the input capacitance, the results are encouraging. Therefore, the preamplifier performance is in agreement with the initial specifications

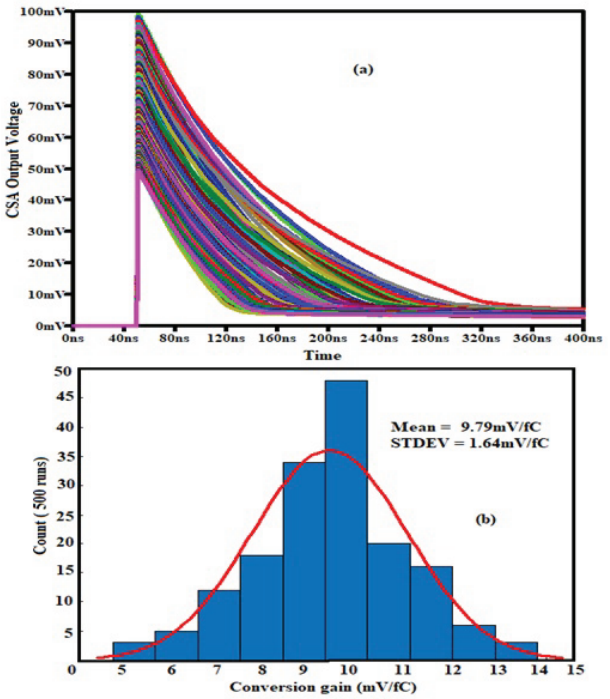

Figure 15: Post-layout Monte-Carlo simulation results (a) Output voltage (b) Conversion gain.

required. On the one hand, the design of the input and feedback transistors allowed us to achieve high linearity, wide bandwidth and sufficient low noise to ensure the good resolution of the below-threshold part of the spectrum in [26]. On the other hand, the optimization of Ibias helps to control the dc gain of the circuit and avoid saturation of the device. Operational Amplifier stability has been guaranteed with a 53.8 dB minimum dc-gain.

4 Conclusions

In this research, a 0.35 µm low-noise stable CSA circuit has been designed for Silicon detector applications.

Table 4: CSA performance summery and comparison.

Parameter	This Work	[5]	[8]	[17]	[21]	[10]
CMOS Technology	0.35 µm	0.35 µm	0.13 µm	0.13 µm	0.35 µm	0.18 µm
Power Supply	3.3 V	1.65 V	1.8 V	1.2 V	3.3 V	1.8 V
Power Consumption	0.23 mW	0.165 mW	1.1 mW	4.8 mW	--	2.1 µW
Input Parasitic Capacitance	0.2 pF – 2 pF	2 pF	15 pF	5 pF	10 pF	--
ENC	42.5 e + 3.72 e/pF	254 e- +13.5 e/pF	418 e	600 e + 100 e/pF	650 e	--
Amplifier Gain	9.92 mV/fC	2.81 mV/fC	0.5 mV/fC	10 mV/fC	15 mV/fC	0.8 µV/fC
Active area (mm^2)	0.0049	0.004212	--	0.7225	0.75	0.038
Input Dynamic Range	0– 480 fC	0 – 120 fC	--	0 – 60 fC	80 fC	150 pC – 450 pC

As per CSA, design requirements, the detector capacitance and the input stage transistor aspect ratio have been optimized in order to achieve the possible low noise and high gain performance. Moreover, adopting NMOS feedback voltage-controlled resistor technique, parallel noise that could be generated by the feedback resistance is removed which in turn ensures high stability of the design. This CSA operates at the amplification of 53.8 dB and works up to 1.023 GHz. It achieved a Charge-Voltage Conversion Factor of 9.92 mV/fC, which is compatible with the state-of-the-art. With a supply voltage of 3.3 V, it dissipates very low power of 0.23 mW. Furthermore, the proposed CSA active die area is only 0.0049 mm2. The satisfactory linearity of this circuit could be used to improve the energy resolution of X-ray radiation detection systems. The achieved results make the proposed CSA a compatible candidate for multi-channel front-end readout ASIC for Silicon detectors applications.

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6 Conflict of Interest

The authors declare no conflict of interest. Besides, the founding sponsors had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, and in the decision to publish the results.

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A Compact 20GHz Dynamic Latch Comparator in 65nm CMOS Process

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***Abstract* —This work reports techniques for designing an ultra-high speed dynamic latch comparator. The effective transconductance of the cross-coupled devices consisting the latch mechanism has been improved using a compact architecture, then reducing mismatch and parasitic, increasing therefore the regeneration speed. The pre-charge step of the preamplifier has been speeded-up using an enhanced differential pair amplifier based active NMOS load. Monte-Carlo analysis of the proposed circuit implemented in 65nm CMOS process, proved that the device can achieve 20GHz sampling frequency while consuming only 78µW of power from 1V supply voltage. The high-speed behavior of the circuit was guaranteed with 14.28ps time delay and 4.45mV offset voltage. The compact circuit layout occupied only 133.15μm^2 of active area.**

Keywords —propagation delay, latch systems, kickback noise power dissipation.

I. INTRODUCTION

High-speed analog to digital converters (ADCs) are frequently used to handle data conversion and signal transmission in communication systems, microprocessors, microcontrollers and FPGA devices. The strap between analog and digital processing methods requires the usage of accurate and low-power ADCs. Variety of communications systems such as Ethernet, wireless communication still need miniaturized and power-efficient mixed signal circuits [1] – [4].

Mixed-mode signal circuits are greatly affected by mismatch and process variations [1], [3], [4]. High frequency (> 1GHz) operations, exacerbate the situation. The main mixed-mode parts circuits of the ADC greatly affected by this concern is the comparator. For high-speed and low-power purpose, latch type comparators are preferred to static counterpart, since their positive feedback enhances the comparison process and the decision making of the latch [5] – [9]. As illustrated on Fig.1, the important role of a latch type comparator is exhibited in the block diagram of a sigma-delta analog to digital converter (ADC).

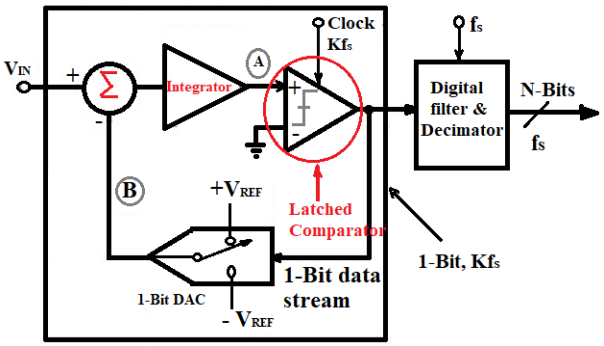

Figure.1. Block diagram of a sigma-delta ADC

The main inconvenient in latch type voltage sense amplifier is the static power dissipation which worsen with scaling down of technology [9]. Besides, input common mode voltage [10] – [12] strongly influences, the operation's speed and offset of the circuit. Reducing offset involves enlarging the devices, increasing the parasitic capacitance, which in turns slows the regeneration process, increases power dissipation therefore and occupies more space [11], [10]. These are the most challenges while implementing high-speed dynamic latched comparator (DLC).

In this research, a compact two stages latch type comparator is designed for ultra-high speed ADCs. The proposed circuit was implemented in 65nm CMOS process using LTSpice and Electric VLSI tools.

II. DESIGN METHODOLOGY

A. The proposed latch type comparator

A custom differential pair amplifier is used as preamplifier stage. The circuit works based on active NMOS load resistor as illustrated in Fig.2 (dotted rectangle). This allows driving a maximum output voltage of V_{DD} - V_{THN} when the drain and gate of the NMOS load devices are settled to V_{DD}. The output terminals of the differential pair should be pre-charged from 0 to V_{DD} - V_{THN} therefore; ensuring a fast comparison speed at this stage. The threshold voltage shifting was minimized thanks to custom transistor design that reduced the body effect which affects the comparison process in the preamplifier module. The proposed compact dynamic latch comparator works in two main steps: the pre-charge step and the regeneration one.

1. *The pre-charge step*

When the clock is low; no current flows through the tail transistor of the sense amplifier (M1), since the device is off. No static power is therefore consumed by the circuit in this state. Transistors M5 and M4 are switched ON, driving therefore nodes F1 and F2 to V_{DD} -V_{THN}; which in turn helps in switching M6 and M7 ON. In addition transistors M8 and M9 behave as an open circuit, then M6 and M7 are turned ON; involving terminals D1 and D2 to be discharged to ground state. Then, the latch outputs are pre-charged to V_{DD} due to the action of the pull-up transistors (M15 and M14) which are switched ON.

2. *The regeneration step*

During the regeneration process, transistors M5, M4, M15, M14, M17 and M16 are switched Off; giving therefore the possibility to transistors M10 and M11 to drive their drain-source current respectively. Currents I_{F1} and I_{F2} flow from V_{DD} to ground; enabling therefore current Icm to flow which helps in turning ON the tail transistor of the sense amplifier. Thanks to the highest transconductance of M2 comparing to M3, the drain's potential of M2 decreases at a faster speed than the drain of M3 when *Vinp>Vinm*. The cross-coupled mechanism of M13/M10 exhibits a positive feedback that kicks in, enabling therefore terminal D1 to drop faster and pulling Voutm to low logic; in the same time M12 is switched ON and pulls Voutp to high logic, the decision is therefore made. Ones the decision made, M10 and M11 are turned off, that avoid static power dissipation [2]. When *Vinp<Vinm,* the opposite phenomena is produced, allowing Voutp to settle low logic and Voutm to high logic. The design of M1 should be therefore of high interest to minimize Icm and prevent dynamic power dissipation of the circuit. The transient induced kickback noise at the regeneration nodes D1 and D2 is reduced thanks to switches M6 and M7 which in turn isolate the drains of the differential input transistors from D1 and D2 during the regeneration phase [2]. The outputs swing of the circuit when its inputs are very close to the latch's trip point is presented in Fig.3. The circuit works slowly and inters in a metastable state, since the differential input voltage of only 5mV is very close to the comparator's input-referred offset. Accordingly, the comparator would not settle a valid level. That phenomenon known as meta-stability, occurs in latch type comparator when the input is near the comparator's decision point. [2], [4]-[8].

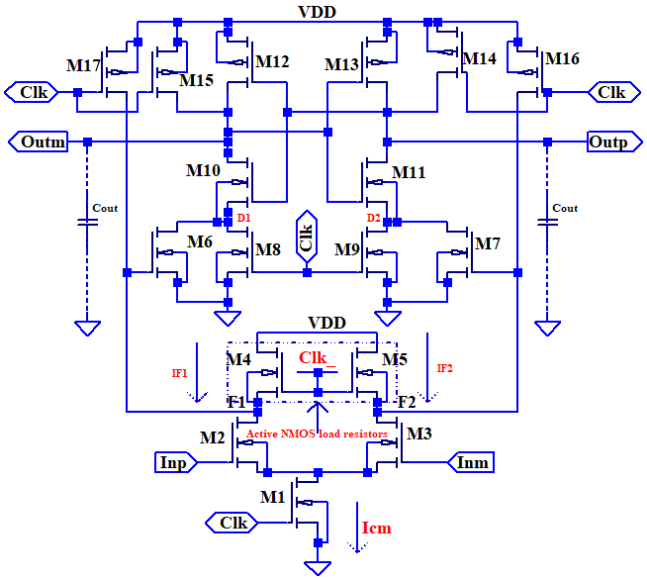

Figure.2. Block diagram of our DLC.

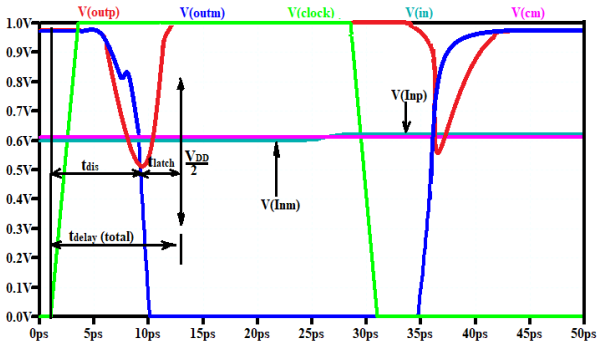

Figure.3.Transient simulation of the proposed dynamic latch comparator (VDD =1V, Vcm= 0.5V, ΔVin = 5mV, clk= 20GHz).

III. RESULTS AND DISCUSSION

A. *Simulation outcomes*

The circuit has been designed and simulated with respect to the 65nm CMOS technology. Fig.4 shows the simulated power-delay product (PDP) of the proposed comparator versus common mode voltage for different differential input voltages. As shwon in Figure.4, when the common mode voltage is larger than 0.6V, the circuit achieved the optimal

design parameters in term of power consumption and time delay. In Fig.5, the average power conmsumption of the proposed circuit is simulated along with the comparator output voltages (Voutp and Voutm). From 1V supply voltage, the circuit consumes only 78 µW of power while operating at 20GHz sampling frequency; the differential input voltage being set to 20mV and the common-mode voltage to 0.5V.

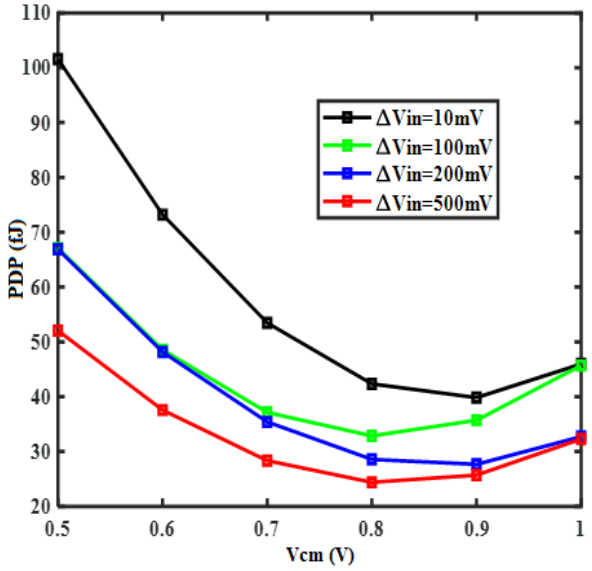

Figure.4. Power delay product of our DLC versus differential input voltage

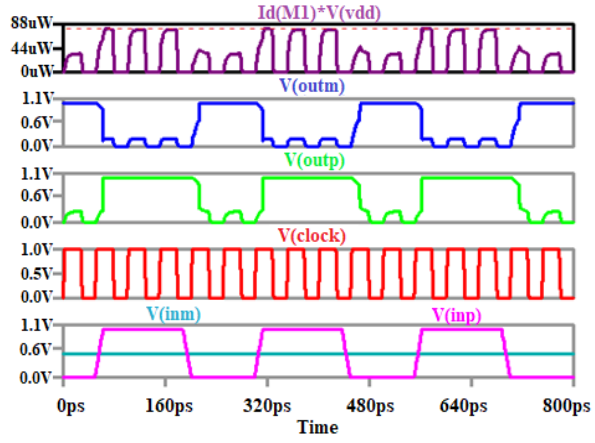

Figure.5.Power consumption of our DLC (VDD =1V, Vcm= 0.5V, ΔVin = 20mV, clk= 20GHz)

B. *Monte-Carlo Simulation*

The transient simulation provided by Monte-Carlo analysis is presented in Fig.6; it clearly reveals that at 20GS/s sampling rate, the proposed DLC's outputs swing do not vary significantly for 500runs. The stability of our circuit has been verified through Monte-Carlo simulation for 500 runs. The latch outputs voltages vary from 0 to $V_{DD} - 62.08mV > \frac{V_{DD}}{2}$ (for Outp) and from 0 to $V_{DD} - 71.13mV > \frac{V_{DD}}{2}$ (for Outm) respectively for 500 runs. As depicted on Fig.6, error due to process variation on Voutp and Voutm is 62.08mV and 71.13mV respectively.

These little variations do not affect the decision of the latch system; confirming therefore the 20GHz clock frequency for ultra-high speed operations respectively when ΔVin = 0.5V, Vcm = 0.5V and the sampling rate being set to 20GHz while using 1V supply voltage. From this statistical analysis, the comparator's offset voltage was reduced to 4.45mV with 3.74mV standard deviation as illustrated on Fig.7. In addition, an average delay time of only 14.28ps with 1.82ps standard deviation was controlled as shown on Fig.8.

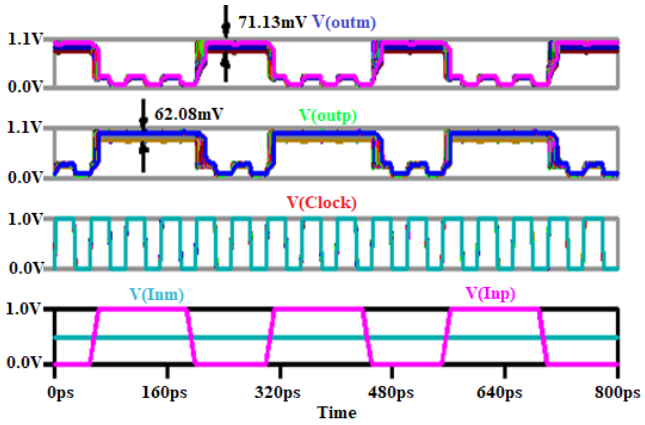

Figure.6. Monte-Carlo simulation results of our DLC for 500 runs.

The proposed design exhibited 8ps time delay during the regeneration process, which involves faster comparison speed. Thanks to the auxiliary transistors, the comparison process is speeded-up by a factor of 33% comparing to that of the circuits proposed in refs [1] and [4]. In Figure.9, the chip layout was designed and a very less die area of 133.15 µm^2 has been achieved, due to mismatch and parasitic reduction during the design process, and mostly to the symmetrical placement of all the MOSFETs consisting the circuits. The transistors have been rigorously sized and their optimal aspect ratios are given in Table.1. This allows achieving accurate and efficient dynamic performance.

C. *Dynamic performance*

The dynamic performance is evaluated by calculating the effective number of bit (ENOB) [11, 12]. Thanks to the smallest input-referred offset (V_{off}) extracted from simulation results, the ENOB is derived from (1) as:

$$V_{off} = \frac{V_{ref}}{2^{ENOB}} \quad (1)$$

where, $V_{ref} = V_{cm} = \frac{V_{DD}}{2}$ was considered for offset simulation with 20Gs/s sampling rate. The ENOB was calculated to be 6.8. Then, a metric applied to latch type comparators and defined as figure of merit (FOM) is used to compare this research with recent state-of-art publications [7]-[10].

$$FOM = \frac{P_d}{2^{ENOB} F_s} \text{ (J/conversion)} \qquad (2)$$

where, Pd is the power consumption of the circuit and F_s being the maximum clock frequency. Based on (2) the FOM was controlled at 0.035fJ/Conversion. That parameter is very important while designing dynamic latch comparator, since the lower the FOM, the higher the efficiency of the circuit [11, 12].

Table.1: Optimized transistors aspect ratio

Transistors	W/L(μm)	Transistors	W/L(μm)
M12,14	0.065/0.065	M1	6.7/0.065
M13,10,11	2/0.065	M2	2.8/0.065
M6	1/0.1	M3	2.8/0.13
M7	0.1/0.1	M4	0.4 /0.32
M15	0.5/0.13	M5	0.1/0.32
M17,16	0.065/0.1	M8,9	3.2/ 0.065

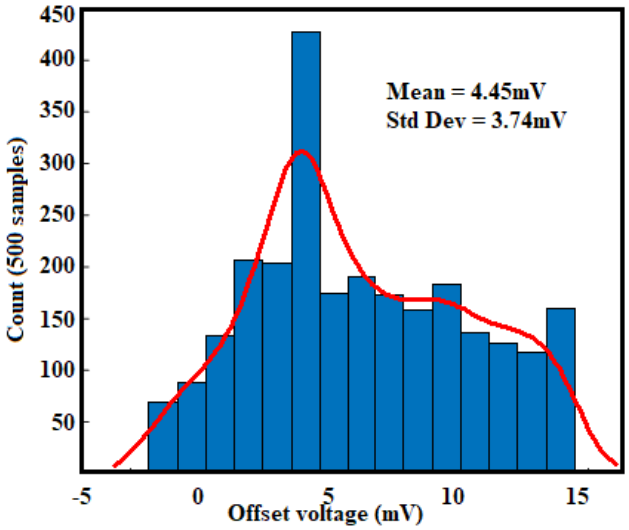

Figure.7. Histogram of the delay extracted from the Mont-Carlo simulation results for 500 runs.

In Table.2, the performance metric of the proposed circuit is highlighted and compared with preceding existing topologies based on simulation. Thanks to the 65 nm CMOS process, we customized a dynamic latch type comparator that achieved 20 GHz sampling rate and consumed only 78 μW of power from 1V supply voltage. Moreover, a less power delay product (PDP) of only 1.114fJ was achieved.

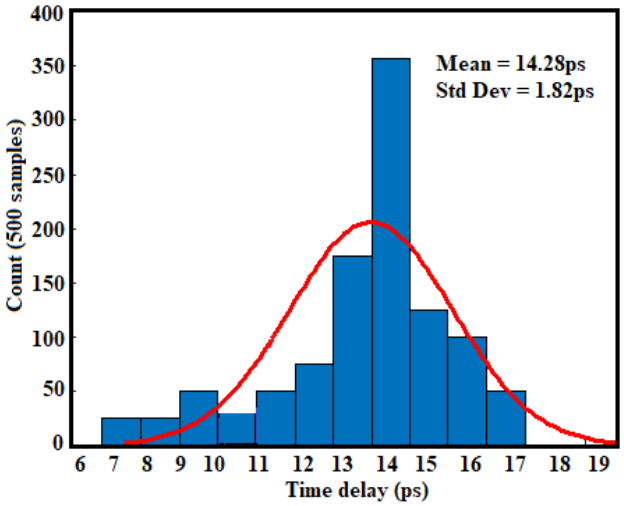

Figure.8. Histogram of the offset extracted from the Mont-Carlo simulation results for 500 runs.

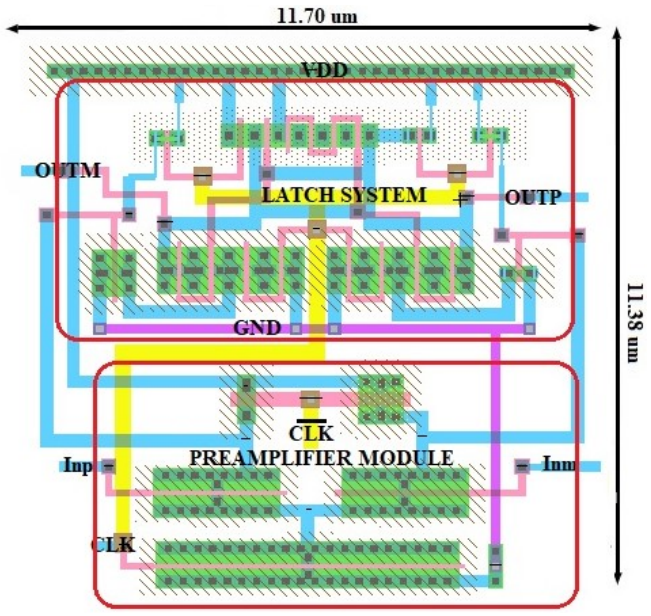

Figure.9. Core circuit layout of our proposed DLC

Table.2: Performance metric of the proposed DLC.

Comparison Properties	[1] 2019	[10] 2019	[4] 2019	[5] 2019	This work
Technology	65nm	180nm	180nm	45nm	65nm
Supply voltage	1.2V	1.8V/ 3.3V	1.8V	0.8V	1V
clock Frequency (GHz)	6	0.625	0.5	14.7	20
Delay (ps)	42.7	N.A	638.91	268	14.28
Power (μW)	381	450	347	5.8	78
Offset (mV)	3.87	0.35	7.78	3.16	4.45
PDP (fJ)	16.3	N.A	221.7	1.55	1.114
FOM (fJ/conversion)	N.A	1.02	N.A	N.A	0.035
Die area (μm^2)	141.7	360	361	26.92	133.15

IV. CONCLUSION

An ultra-high speed dynamic latch comparator has been implemented in this work. The parasitic and mismatch were reduced in the latch stage and the circuit was isolated to ground using auxiliary transistors, which gave a compact architecture to the design. The effective transconductance of cross-coupling inverter of the latch mechanism was improved therefore increased the speed of our circuit. The implementation has been carried out using 65nm CMOS process from TSMC. A maximum clock frequency of 20GHz was achieved and the circuit exhibited an acceptable PDP of 1.114fJ per clock cycle, while a lower input referred-offset of 4.45mV was achieved.

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